agere systems

Data Sheet
July 2001

L9312 Line Interface and Line Access Circuit Forward Battery SLIC and Ringing Relay for TR-57 Applications

Introduction

The Agere Systems Inc. L9312 is a combination full-feature, ultralow-power SLIC, and solid-state ringing access relay. It is part of a pin-for-pin compatible family of devices designed to serve a wide variety of applications. The L9312 is optimized for TR-57 access, forward battery only, applications.

Features

SLIC

- 5 V and battery operation
- Optional automatic battery switch
- Four operational modes
- Appropriate for 58 dB longitudinal balance applications
- Minimal external components required at all interfaces
- Ultralow power dissipation
- Software/hardware adjustable dc parameters and supervision thresholds

Solid-State Ring Relay

- Low impulse noise
- Current-limited switches/thermal protection

Applications

- Pair Gain
- Digital Loop Carrier (DLC)
- Central Office (CO)
- Fiber-in-the-Loop (FITL)

Description

The L9312 electronic line interface and line access circuit (LILAC) provides all the functions that are necessary to interface a codec to the tip and ring of a subscriber loop, integrating the battery feed and ringing access relay in one low-power, low-cost package.

The L9312 requires a 5 V and battery supply to operate. Included is an automatic battery switch. The battery feed offers forward battery and on-hook transmission. It also has a low-power scan and a disconnect mode.

In all operating states, this IC is designed for minimal power dissipation. This device is designed to minimize the number of external components required at all interfaces.

The dc template, current limit, and overhead voltage and loop supervision threshold are programmable via an applied voltage source. The voltage source may be an external programmable voltage source or derived from the V_{REF} SLIC output.

The integrated solid-state switch offers power ringing access. Impulse noise is minimized, thus eliminating the need for external zero-cross switching circuitry.

Table of Contents

Table of Contents (continued)

Figures

Tables

Features

- SLIC and solid-state ring relay integrated into a single package
- 5 V and battery operation
- User-defined power control options:
  — Automatic battery switch
  — Power control resistor
  — Package thermal capabilities
- Minimal external components required
- Operating states:
  — Forward active
  — Scan
  — All-off or disconnect
  — Ring
- Ultralow power:
  — Scan, 15 mW
  — Active states, on-hook, 75 mW
  — Ring mode, on-hook, 90 mW
  — Disconnect, 10 mW
- Adjustable overhead voltage:
  — Default overhead adequate for 3.14 dB into 900 Ω overload
  — Controlled rate of overhead adjustment
- Latched parallel input data interface with reset
- Adjustable current limiter:
  — 10 mA to 45 mA programming range
- Adjustable loop closure detector with hysteresis:
  — 4 mA detect, 2.5 mA no detect minimum, upper limit of 15 mA detect
  — Hysteresis, typical 20% of programmed on-hook to off-hook threshold
- Ring trip detector:
  — Single-pole filtering
- Thermal shutdown protection with hysteresis
- Line break switch will foldover into a low-current state under high-voltage fault conditions
- Battery out-of-range monitor circuit:
  — All-off upon loss of battery (low battery condition)
  — All-off upon high battery (fault condition)
- Longitudinal balance:
  — TR-57 balance
- RFI/EMC-CISP-22
- Integrated 2 Form C ring relay:
  — Low impulse noise
  — Current-limited switches
  — Break-before-make and make-before-break switching
- Meets *Telcordia Technologies** GR1089 requirements with external protection device
- 44-pin, surface-mount plastic package (PLCC)

Description

The L9312 electronic line interface and line access circuit (LILAC) provides all the functions that are necessary to interface a codec to the tip and ring of a subscriber loop, integrating the battery feed and ringing access relay in one low-power, low-cost package. The physical construction of the device is two chips. The first chip is manufactured in Agere 90 V complementary bipolar integrated circuit (CBIC-S) technology. This chip contains the SLIC functionality:

- ac transmission path
- dc feedback and functions
- Active dc current limit
- Active mode loop supervision
- Thermal shutdown

The second chip is manufactured in Agere dielectrically isolated 320 V bipolar CMOS diffused metal oxide semiconductor (BCDMOS III) technology. This chip contains the following:

- Ring access relay
- Scan clamp circuitry
- Logic control
- Ring trip
- Thermal shutdown
- Battery monitor circuit

The LILAC family requires a +5 V and battery supply to operate. No –5 V supply is required. A battery switch is included that automatically, based on subscriber loop length, will apply either the primary higher-voltage battery or an optional lower-voltage auxiliary battery. Use of this feature will minimize off-hook power dissipation.

* *Telcordia Technologies* is a trademark of Bell Communications Research, Inc.

Description (continued)

The switch point is a function of the user-programmed dc current limit and the magnitude of the auxiliary battery. Switching from the high-voltage to low-voltage battery is quiet, without interruption of the dc loop current, thus preventing any impulse noise generation at the switch point. Design equations for the switch point and a graph showing loop/battery current versus loop resistance are given in the dc Characteristics in the Applications section of this data sheet.

If the user does not want to provide an auxiliary battery, the design of the L9312 battery switch allows use of a power control resistor at the auxiliary battery input. This scheme will not reduce short-loop, off-hook power dissipation, but it will control power dissipation on the SLIC by sharing power among the SLIC, power resistor, and dc loop. However, in most cases, without the auxiliary battery, the power dissipation capabilities of the 44-pin PLCC package are adequate so that the power control resistor will not be needed. Design equations for power control options are given in the dc Characteristics section of this data sheet.

The L9312 is a forward battery only SLIC that supports on-hook transmission.

A low-power scan mode is available to reduce idle mode on-hook power. This mode is realized by using a scan clamp circuit. In low-power scan mode:

- The scan clamp circuitry is active.
- Loop closure is active.
- All ac transmission, dc feed, and other supervision circuits, including ring trip, are shut down.
- Thermal shutdown is active.
- Low battery sense shutdown is on.
- On-hook transmission is disabled.

A forward disconnect mode, where all circuits are turned off and power is denied to the loop, is also provided. During this mode, the NSTAT supervision output will read on-hook.

In the ring mode, the line break switches are opened and the power ring access switches are closed. In this mode, the ring trip detector in the SLIC is active and all other detectors and the tip/ring drive amplifiers are turned off to conserve power.

Make-before-break or break-before-make switching is achievable during ring cadence or ring trip. Toggling directly into or directly out of the ring mode table will give make-before-break switching. To achieve break-before-make switching, go to an intermediate all-off state (use forward disconnect state) before entering the ring mode or before leaving the ring mode. See the Switching Behavior section of this data sheet for more details on switching behavior.

Voltage transients or impulse noise associated with ring cadence or ring trip are minimized or eliminated with the L9312, thus possibly eliminating the need for external zero-cross switching circuitry.

Both the ring trip and loop closure supervision functions are included. Loop closure threshold is set by applying a voltage source to the LCTH input. The voltage source may be an external voltage source or derived from the SLIC V_{REF} output. A programmable external voltage source may be used to provide software control of the loop closure threshold. Design equations for the loop closure threshold are given in the Supervision section of this data sheet. Hysteresis is included.

The ring trip detector requires only a single-pole filter at the input. This will minimize the required number of external components. To help minimize device power dissipation, the ring trip detector is active only during the power ring mode.

Ring trip and loop supervision status outputs appear in a common output pin, NSTAT. NSTAT is an unlatched supervision output; thus, an interrupt-based control scheme may be used.

The dc current limit is set in the active modes via an applied voltage source. The voltage source may be an external voltage source. The voltage may be derived via a resistor divider network from the V_{REF} SLIC output. A programmable external voltage source may be used to provide software control of the loop closure threshold. Design equations for this feature are given in the dc Characteristics section of this data sheet. Programming range is 10 mA to 45 mA.

Overhead is programmable in the active modes via an applied voltage source. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output.

A programmable external voltage source may be used to provide software control of the overhead voltage. The rate of change of the overhead voltage may be controlled by use of a single external capacitor at the C_{F1} node. If the rate of change is uncontrolled, there may be audible noise associated with this transition. Design equations for this feature are given in the dc Characteristics section of this data sheet.

If the overhead is not programmed via a resistor, the device develops a default overhead adequate for a 3.14 dBm overload into 900 Ω. For the default overhead, OVH is connected to ground.

Description (continued)

Data control is via a parallel latched data control scheme. Data latches are edge-level sensitive. Data is latched in when the LATCH control input goes low. While LATCH is low, the user cannot change the data control inputs. The data control inputs may only be changed when LATCH is high.

Incorporation of data latches allows for data control information and loop supervision information to be passed to and from the SLIC via data buses rather than on a per-line basis, thus minimizing routing complexity and board routing area.

A device RESET pin is included. When this pin is low, the logic inputs are overridden and the device will be reset into SLIC forward disconnect state and the switch into the all-off state. NSTAT is forced to the on-hook condition when RESET is low.

The overall device protection is achieved through a combination of an external secondary protector, along with an integrated thermal shutdown feature, a battery voltage window comparator, the break switch foldback characteristic, and the dc/dynamic current-limit response of the break and tip return switches.

For protection against long duration fault conditions, such as power cross and tip/ring shorts, a thermal shutdown mechanism is integrated into the device. Upon reaching the thermal shutdown temperature, the device will enter an all-off mode. Upon cooling, the device will re-enter the state it was in prior to thermal shutdown. Hysteresis is built in to prevent oscillation. During this mode, the NSTAT supervision output overrides the actual loop status and forces an off-hook.

The line break switches and tip return switch are current-limited switches. The current-limit mechanism limits current through the switch to the specified dc current limit under low frequency or dc faults (power cross and/or tip/ring to ground short) and limits the current to the specified dynamic current-limit response under transient faults, such as lightning.

A foldover characteristic is incorporated into the line break switches within their I-V curve. Under voltage conditions higher than the normal operating range, such as may be seen under an extreme lightning or power cross fault condition, the line break switch will fold over into a low-current state. This feature allows for more relaxed specifications on the ring side protector, thus allowing for higher-voltage ringing signals. (Tip side protector is limited by the requirements on the tip return switch.) This feature is part of the overall device protection scheme.

This device uses a window comparator to force an all-off condition if the battery drops below, or rises above, a specified threshold.

Upon loss of V_{BAT1}, the L9312 will automatically enter an all-off mode. The device will enter this mode if the magnitude of the battery drops below a nominal 15 V and will remain in this mode until the magnitude of the battery rises above a typical 20 V. During this mode, the NSTAT supervision output will override the actual hook status and force an off-hook or logic low.

When the device is in the scan mode, because of the design of the scan clamp circuit, common-mode current can be forced into or out of the battery supply. Because of this, and depending upon power supply design, the magnitude of the battery may rise above the maximum operating condition during extended longitudinal currents or during a power cross fault condition. To prevent excess current from being forced into or out of the battery, if the magnitude of the battery rises typically above 75 V to 80 V, the device will enter an all-off state. The device will remain in the all-off state until the magnitude of the battery drops into the normal operating range. During this mode, the NSTAT supervision output will override the actual hook status and force an off-hook or logic low.

See the Protection section of this data sheet for more details on device protection. Please contact your Agere Account Representative for a recommended secondary protection device.

Longitudinal balance is consistent with North American TR-57 requirements.

Transmit and receive gains have been chosen to minimize the number of external components required in the SLIC-codec ac interface, regardless of the choice of codec.

The L9312 uses a voltage feed, current sense architecture; thus, the transmit gain is a transconductance. The L9312 transconductance is set via a single external resistor, and this device is designed for optimal performance with a transconductance set at 300 V/A.

The L9312 offers an option for a single-ended to differential receive gain of either 8 or 2. These options are mask programmable at the factory and are selected by choice of part number.

A receive gain of 8 is more appropriate when choosing a first-generation type codec where termination impedance, hybrid balance, and overall gains are set by external analog filters. The higher gain is typically required for synthesization of complex termination impedance.

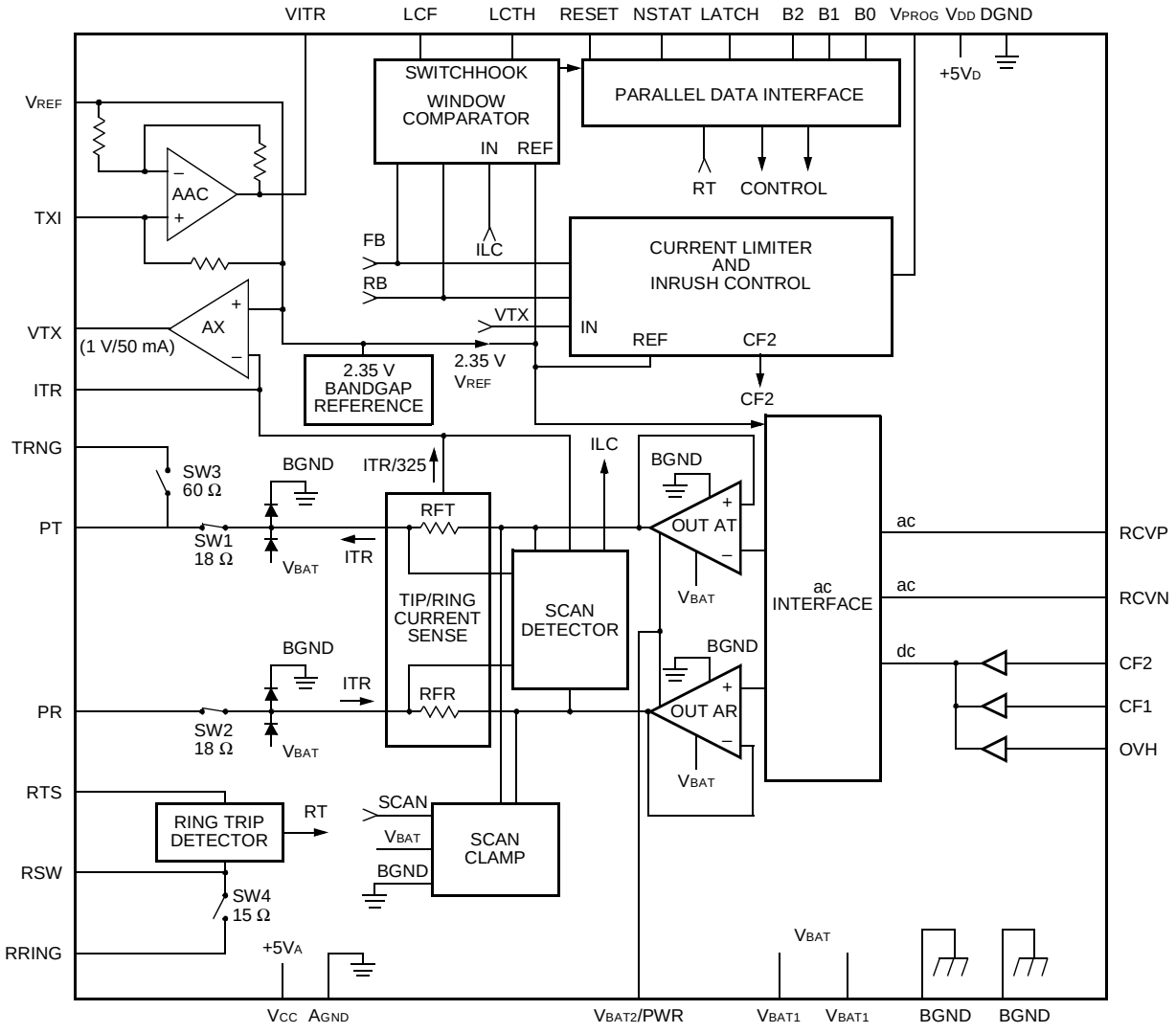
Description (continued)

A receive gain of 2 is more appropriate when choosing a third-generation type codec. Third-generation codecs will synthesize termination impedance, set hybrid balance, and set overall gains. To accomplish these functions, third-generation codecs typically have both analog and digital gain filters. For optimal signal-to-noise performance, it is best to operate the codec at a higher gain level. If the SLIC then provides a high gain, the SLIC output may be saturated causing clipping distortion of the signal at tip and ring. To avoid this situation, with a higher-gain SLIC, external resistor dividers are used. These external components are not necessary with the lower gain offered by the L9312.

The RCVP/RCVN SLIC inputs are floating inputs. If there is not feedback from RCVP/RCVN to VITR, RCVP/RCVN may be directly coupled to the codec output. If there is feedback, RCVP/RCVN must be ac-coupled to the codec output.

This device is packaged in a 44-pin PLCC surface-mount package.

Architecture



12-3523e (F)

Figure 1. Architecture Diagram

Pin Information

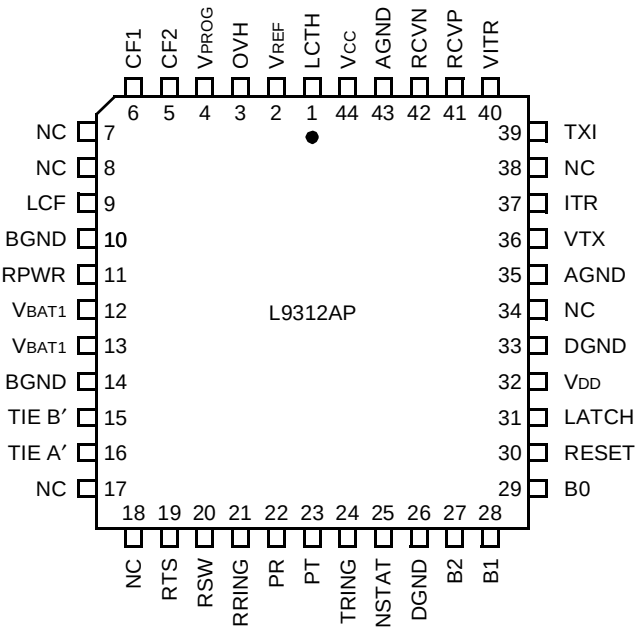


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Figure 2. 44-Pin PLCC

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	LCTH	I	**Loop Closure Program Input.** Connect a voltage source to this point to program the loop closure threshold. Voltage source may be external and must be connected through a resistor, or derived via a resistor divider from V_{REF}. A programmable external voltage source may be used to provide software control of the loop closure threshold.
2	V_{REF}	O	**SLIC Internal Reference Voltage.** Output of internal 2.35 V SLIC reference voltage.
3	OVH	I	**Overhead Voltage Program Input.** Connect a voltage source to this point to program the overhead voltage. Voltage source may be external or derived via a resistor divider from V_{REF}. A programmable external voltage source may be used to provide software control of the overhead voltage. If a resistor or voltage source is not connected, the overhead voltage will default to approximately 5.5 V (sufficient to pass 3.14 dBm in to 900 Ω). If the default overhead is desired, connect this pin to ground.
4	V_{PROG}	I	**Current-Limit Program Input.** Connect a voltage source to this point to program the dc current limit. Voltage source may be external or derived via a resistor divider from V_{REF}. A programmable external voltage source may be used to provide software control of the loop closure threshold.
5	CF2	—	**Filter Capacitor.** Connect a capacitor from this node for filtering.
6	CF1	—	**Filter Capacitor.** Connect a capacitor from this node to OVH to control the rate of change of the overhead voltage. If controlled overhead is not desired, leave this node open.
7, 8, 17, 18, 34	NC	—	**No Connect.** May not be used as a tie point.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
9	LCF	—	**Loop Closure Filter Capacitor.** PPM injection can cause false loop closure indication. Connect a capacitor from this node to V_{CC} to filter the loop closure detector. If loop closure filtering is not required, leave this node open.
10	BGND	G	**Battery Ground.** Ground return for the battery supply.
11	RPWR	P	**Auxiliary Battery.** If a lower-voltage auxiliary battery is used, connect the auxiliary battery supply to this node. If a power control resistor is used, connect the power control resistor from this node to V_{BAT1}. If no power control technique is used, connect this node to V_{BAT1}.
12	V_{BAT1}	P	**Office Battery Supply.** Negative high-voltage power supply.
13	V_{BAT1}	P	**Office Battery Supply.** Negative high-voltage power supply.
14	BGND	G	**Battery Ground.** Ground return for the battery supply.
15	TIE B’	—	**Connect to V_{REF}.**
16	TIE A’	—	**Connect to V_{REF}.**
19	RTS	I	**Ring Trip Sense.** Sense input for the ring trip detector.
20	RSW	O	**Ring Lead Ringing Access Switch.** Ringing relay connects this pin to pin RRING. Connect this pin to pin PR through a 400 Ω current-limiting resistor.
21	RRING	I	**Ringing Access.** Input to solid-state ringing access switch. Connect to ringing generator.
22	PR	I/O	**Protected Ring.** The output of the ring driver amplifier and input to loop sensing connected through solid-state break switch. Connect to subscriber loop through overvoltage/current protection.
23	PT	I/O	**Protected Tip.** The output of the tip driver amplifier and input to loop sensing connected through solid-state break switch. Connect to subscriber loop through overvoltage/current protection.
24	TRING	O	**Tip Ringing Return.** Ring relay connects this pin to PT. Connect to ringing supply return.
25	NSTAT	O	**Loop Status.** The output of the loop status detector (loop start detector wired-OR with ring trip detector). This loop status supervision output is not controlled by the data latch.
26	DGND	G	**Digital Ground.** Ground return for V_{DD} current.
27	B2	I	**Data Control Input.** See Table 2, Control States, for details.
28	B1	I	**Data Control Input.** See Table 2, Control States, for details.
29	B0	I	**Data Control Input.** See Table 2, Control States, for details.
30	RESET	I	**Reset.** A logic low will override the B[0:3] and LATCH inputs and reset the state of the SLIC to the disconnect state and the switch to the all-off state.
31	LATCH	I	**Latch Control Input.** Edge-level sensitive control for data latches.
32	V_{DD}	P	**5 V Digital Power Supply.** 5 V supply for digital circuitry.
33	DGND	G	**Digital Ground.** Ground return for V_{DD} current.
35	AGND	G	**Analog Ground.**
36	VTX	O	**Tip/Ring Voltage Output.** This output is a voltage that is directly proportional to the differential tip/ring current. A resistor from this node to ITR sets the device transimpedance. Gain shaping for termination impedance with a COMBO I codec is also achieved with a network from this node to ITR.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	Type	Name/Function
37	ITR	I	**Transmit Gain.** A current output which is proportional to the differential current flowing from tip to ring. Input to AX amplifier. Connect a resistor from this node to VITR to set transmit gain to 300 Ω. Gain shaping for termination impedance with a COMBO I codec is also achieved with a network from this node to VITR.
38	NC	—	**No Connect.** May not be used as a tie point.
39	TXI	I	**Transmit ac Input (Noninverting).** Connect a 0.1 μF capacitor from this pin to VTX for dc blocking.
40	VITR	O	**Transmit ac Output Voltage.** The output is a voltage that is directly proportional to the differential ac tip/ring current. This output is connected via a proper interface network to the codec.
41	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on tip and ring.
42	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on tip and ring.
43	AGND	G	**Analog Ground.** Ground return for V_{CC} current.
44	V_{CC}	P	**5 V Analog Power Supply.** 5 V supply for analog circuitry.

Operating States

Input State Coding

Data control is via a parallel latched data control scheme. Data latches are edge-level sensitive. Data is latched in when the LATCH control input goes low. Data must be set up 200 ns before LATCH goes low and held 50 ns after LATCH goes high. While LATCH is low, the user should not change the data control inputs at B0, B1, and B2. The data control inputs at B0, B1, and B2 may only be changed when LATCH is high. NSTAT supervision output is not controlled by the LATCH control input.

Table 2. Control States

B2	B1	B0	RESET	State
0	0	0	1	Scan
0	0	1	1	Powerup, forward battery
0	1	0	1	Unassigned
0	1	1	1	Unassigned
1	0	0	1	Ring
1	0	1	1	Unassigned
1	1	0	1	Unassigned
1	1	1	1	Disconnect, break before make
X	X	X	0	Disconnect, break before make

Table 3. Supervision Coding

Pin NSTAT	Pin TRGDET
0 = off-hook or ring trip	0 = ring ground
1 = on-hook and no ring trip	1 = no ring ground

State Definitions

Primary Control Modes

Powerup, Forward Battery

- Normal talk and battery feed state.
- Pin PT is positive with respect to pin PR.
- All ac transmission and dc feed circuits are powered up.
- On-hook transmission is enabled.
- Thermal shutdown is active.
- Battery window comparator sense shutdown is on.
- Switch break switches (SW1 and SW2) are closed, and ring access switches (SW3 and SW4) are open.
- V_{BAT1} is applied to tip and ring during on-hook conditions.
- Automatic battery switch selects V_{BAT1} or V_{BAT2} during off-hook conditions.
- All supervision circuits except for ring trip detector are active.
- NSTAT represents the loop closure detector status.

Scan

- Scan clamp circuitry is active.
- Loop closure is active.
- All ac transmission, dc feed, and other supervision circuits, including ring trip, are shut down.
- Thermal shutdown is active.
- Battery window comparator sense shutdown is on.
- On-hook transmission is disabled.
- Pin PT is positive with respect to PR, and V_{BAT1} is applied to tip/ring.
- Switch break switches (SW1 and SW2) are closed, and ring access switches (SW3 and SW4) are open.
- NSTAT represents the loop closure detector status.

Ringing

- Switch break switches (SW1 and SW2) are open, and ring access switches (SW3 and SW4) are closed.
- Tip/ring drive amplifiers are powered down.
- Ring trip circuit is active.
- Loop supervision and common-mode current detectors are powered down.
- NSTAT represents the ring trip detector status.

Disconnect—Break Before Make

- The tip and ring amplifiers are turned off to conserve power.
- Break switches (SW1 and SW2) are open, and ring access switches (SW3 and SW4) are open. This mode is also used as a transitional mode to achieve break-before-make switching from the power ring to active or scan mode.
- All supervision circuits are powered down; NSTAT overrides the actual loop condition and is forced high (on-hook).

Reset

- Selection of device reset via the RESET pin will set the device into the disconnect break-before-make state.

Special States

Thermal Shutdown

- Not controlled via truth table inputs.
- This mode is caused by excessive heating of the device, such as may be encountered in an extended power cross situation.
- Upon reaching the thermal shutdown temperature, the device will enter an all-off mode.
- Upon cooling, the device will re-enter the state it was in prior to thermal shutdown.
- Hysteresis is built in to prevent oscillation. In this mode, supervision output NSTAT is forced low (off-hook) regardless of loop status or if the disconnect logic state is selected.

State Definitions (continued)

Special States (continued)

Battery Out of Range

- Not controlled via truth table inputs.
- This mode is caused by a battery out of range; that is, the battery voltage rising above or below a specified threshold.
- Upon reaching the specified high or low battery voltage, the device will enter an all-off mode.
- Upon the battery returning to the specified normal operating range, the device will re-enter the state it was in prior to the low battery shutdown.
- Hysteresis is built in to prevent oscillation. In this mode, supervision output NSTAT is forced low (off-hook) regardless of loop status or if the disconnect logic state is selected.

Absolute Maximum Ratings (at T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
5 V dc Supplies (V_{CC})	—	–0.5	7.0	V
High Office Battery Supply (V_{BAT1})	—	–75	0.5	V
Auxiliary Office Battery Supply (V_{BAT2})	—	—	V_{BAT1} to 0.5 V	V
Ringing Voltage	—	—	110	Vrms
Logic Input Voltage	—	–0.5	V_{CC} + 0.5 V	V
Maximum Junction Temperature	—	—	165	°C
Storage Temperature Range	—	–40	125	°C
Relative Humidity Range	—	5	95	%
Switch 1, 2, 3; Pole to Pole	—	—	320	V
Switch 4; Pole to Pole	—	—	465	V
Switch Input to Output	—	—	320	V

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. For example, inductance in a supply lead could resonate with the supply filter capacitor to cause a destructive overvoltage.

Electrical Characteristics

In general, minimum and maximum values are testing requirements. However, some parameters may not be tested in production because they are guaranteed by design and device characterization. Typical values reflect the design center or nominal value of the parameter; they are for information only and are not a requirement. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C) and entire battery range (–36 V to –70 V). Unless otherwise specified, typical is defined as 25 °C, V_{CC} = V_{DD} = 5.0, V_{BAT1} = –48 V V_{BAT2} = –25 V. Positive currents flow into the device.

Table 4. Device Operating Conditions and Powering

Parameter	Min	Typ	Max	Unit
Temperature Range	–40	—	85	°C
Humidity Range	5	—	95*	%RH
V_{BAT1} Operational Range	–36	–48	–72	V
V_{BAT2} Operational Range	–19	–25	V_{BAT1}	V
5 V dc Supplies (V_{CC}, V_{DD})	4.75	5.0	5.25	V
Supply Currents, Scan State				
No Loop Current, V_{BAT} = –48 V, V_{CC} = V_{DD} = 5 V:				
I_{VCC}	—	2	2.5	mA
I_{VBAT1}	—	100	200	µA
Power Dissipation	—	15	22	mW
Supply Currents, Forward Active				
No Loop Current, with On-hook Transmission, V_{BAT} = –48 V,				
V_{CC} = V_{DD} = 5 V:				
I_{VCC}	—	6	6.5	mA
I_{VBAT1}	—	1.1	1.4	mA
Power Dissipation	—	83	100	mW
Supply Currents, Forward Disconnect, V_{BAT} = –48 V, V_{CC} = V_{DD} = 5 V:				
I_{VCC}	—	1.2	1.85	mA
I_{VBAT1}	—	65	275	µA
Power Dissipation	—	9	22.5	mW
Supply Currents, Ring State, No Loop Current,				
V_{BAT} = –48 V, V_{CC} = V_{DD} = 5 V, V_{RING} = 80 Vrms:				
I_{VCC}	—	4	—	mA
I_{VBAT1}	—	200	—	µA
I_{RING} Generator	—	500	—	µA
Power Dissipation	—	70	—	mW
PSRR 500 Hz—3000 Hz:				
V_{BAT1}, V_{BAT2}	45	—	—	dB
V_{CC}	30	—	—	dB
Thermal Protection Shutdown (T_{TSD})	150	165	—	°C

* Not to exceed 26 grams of water per kilogram of dry air.

Electrical Characteristics (continued)

Ring Trip Detector

Table 5. Ring Trip Detector

Parameter	Min	Typ	Max	Unit
Voltage at Input that will Cause Ring Trip After Appropriate Zero Crossings	±2.5	±3	±3.5	V
Voltage at Input that will Cause Immediate Ring Trip	±12	±15	±18	V
Ringing Source[1]:				
Frequency (f)	19	20	28	Hz
dc Voltage	–39.5	—	–57	V
ac Voltage	60	—	105	Vrms
Ring Trip (NDET = 0)[2, 3]:				
Loop Resistance	2000	—	—	Ω
Trip Time	—	—	200	ms
NDET Valid	—	—	80	ms

1. The ringing source may be either of the following:
   a.) The ringing source consists of the ac and dc voltages added together (battery-backed ringing); the ringing return is ground.
   b.) The ringing source consists of only the ac voltage (earth-backed ringing); the ringing return is the dc voltage.
2. NDET must also indicate ring trip when the ac ringing voltage is absent (<5 Vrms) from the ringing source.
3. Pretrip ringing must not be tripped by a 10 kΩ resistor in parallel with an 8 µF capacitor applied across tip and ring.

Electrical Characteristics (continued)

SLIC Two-Wire Port

Table 6. SLIC Two-Wire Port

Parameter	Min	Typ	Max	Unit
PT and PR Drive Current = dc + Longitudinal + Signal Currents	70	—	—	mApeak
Signal Current	10	—	—	mArms
Longitudinal Current Capability per Wire (longitudinal current is independent of dc loop current)	8.5	15	—	mArms
dc Active Mode Loop Current – I_{LIM} (R_{LOOP} = 100 Ω):				
Programming Range (5 Vrms max into 200 Ω ac)	10	—	45	mA
Voltage at V_{PROG}	0.2	0	0.9	V
dc Current-limit Variation:				
V_{PROG} = 0.8 V (I_{LIMIT} = 40 mA)	—	5	—	%
Loop Resistance Range (from PT/PR) (3.17 dBm overload into 600 Ω):				
I_{LOOP} = 20 mA at V_{BAT1} = –48 V	1900	—	—	Ω
V_{REF}	2.23	2.35	2.47	V
Offset at V_{PROG}	–40	—	40	mV
dc Feed Resistance (includes internal SLIC dc resistance and break switch resistance)	50	75	110	Ω
dV/dT Sensitivity at PT/PR	—	200	—	V/µs
Powerup Open Loop Voltages (V_{BAT1} = –48 V):				
Forward/Reverse Active Mode |PT – PR| – V_{BAT1}	5.5	—	15	V
Voltage at OVH	0	—	1.9	V
Forward/Reverse Active Mode |PT – PR| – V_{BAT1}, V_{OVH} = 0	5.5	6.1	—	V
Common Mode	—	(V_{BAT1} + 1)/2	—	V
Powerup Open Loop Voltages:				
Scan Mode |PT – PR| – V_{BAT1}	0	—	13.5	V
Loop Closure Threshold:				
Voltage at LCTH	0	—	V_{REF}	V
Loop Closure Threshold Hysteresis	—	20	—	%
Longitudinal to Metallic Balance at PT/PR (Test Method: *IEEE** Std. 455):				
200 Hz to 3.4 kHz	61	—	—	dB
Metallic to Longitudinal (harm) Balance:				
200 Hz to 4000 Hz	40	—	—	dB

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Electrical Characteristics (continued)

Analog Pin Characteristics

Table 7. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
TXP (input impedance)	75	105	—	kΩ
V_{PROG} Input Bias Current* (current flow out of pin)	—	–50	–250	nA
LCTH Input Bias Current* (+ current flows into pin)	—	50	250	nA
VTX:				
Output Offset	—	—	±40	mV
Output Drive Current	±1	—	—	mA
Output Voltage Swing (±1 mA load):				
Maximum	AGND	—	V_{CC}	V
Minimum	AGND + 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current	—	—	±50	mA
Output Load Resistance	10	—	—	kΩ
Output Load Capacitance	—	50	—	pF
VITR:				
Output Offset	—	—	±100	mV
Output Drive Current	±1	—	—	mA
Output Voltage Swing (±1 mA load):				
Maximum	AGND	—	V_{CC}	V
Minimum	AGND + 0.35	—	V_{CC} – 0.4	V
Output Short-circuit Current	—	—	±50	mA
Output Load Resistance	10	—	—	kΩ
Output Load Capacitance	—	50	—	pF
RCVN and RCVP:				
Input Voltage Range (V_{CC} = 5.0 V)	0	—	V_{CC} – 0.5	V
Input Bias Current	—	—	±1.5	µA

* This parameter is not tested in production. It is guaranteed by design and device characterization.

Electrical Characteristics (continued)

ac Feed Characteristics

Table 8. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	600	1400	Ω
Total Harmonic Distortion (200 Hz—4 kHz)[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain[3] f = 1004 Hz, 1020 Hz:				
PT/PR Current to VITR	–291	–300	–309	V/A
Receive Gain, f = 1004 Hz, 1020 Hz Open Loop:				
RCVP or RCVN to PT—PR (gain = 8)	7.76	8	8.24	—
RCVP or RCVN to PT—PR (gain = 2)	1.94	2	2.06	—
ac Feed Resistance (includes internal SLIC ac resistance and break switch resistance)	50	75	110	Ω
Gain vs. Frequency (transmit and receive)[2] 900 Ω = 2.16 µF Termination, 1004 Hz Reference:				
200 Hz—300 Hz	–0.3	0	0.05	dB
300 Hz—3.4 kHz	–0.05	0	0.05	dB
3.4 kHz—20 kHz	–3.0	0	0.05	dB
20 kHz—266 kHz	—	—	2.0	dB
Gain vs. Level (transmit and receive)[2] 0 dBV Reference:				
–55 dB to +3.0 dB	–0.05	0	0.05	dB
Idle-channel Noise (tip/ring) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn
Idle-channel Noise (VTX) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn

1. Set externally either by discrete external components or a third- or fourth-generation codec. Any complex impedance R1 + R2 || C between 150 Ω and 1400 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. VITR transconductance depends on the resistor from ITR to VTX. This gain assumes an ideal 6.34 kΩ, the recommended value. Positive current is defined as the differential current flowing from PT to PR.

Electrical Characteristics (continued)

Logic Inputs and Outputs, V_{DD} = 5.0 V

Table 9. Logic Inputs and Outputs

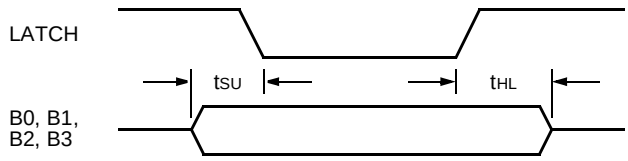
Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.4	0.7	V
High Level	V_{IH}	2.0	2.4	V_{DD}	V
Input Current:					
Low Level (V_{DD} = 5.25 V, V_I = 0.4 V)	I_{IL}	—	—	±50	µA
High Level (V_{DD} = 5.25 V, V_I = 2.4 V)	I_{IH}	—	—	±50	µA
Output Voltages (CMOS):					
Low Level (V_{DD} = 4.75 V, I_{OL} = 180 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{DD} = 4.75 V, I_{OH} = –20 µA)	V_{OH}	2.4	—	V_{CC}	V

Timing Requirements

Table 10. Timing Requirements

Parameter	Symbol	Min	Typ	Max	Unit
Minimum Setup Time from B0, B1, B2 to LATCH	t_{SU}	200	—	—	ns
Minimum Hold Time from LATCH to B0, B1, B2	t_{HL}	50	—	—	ns

Data control is via a parallel latched data control scheme. Data latches are edge-level sensitive. Data is latched in when the LATCH control input goes low. Data must be set up t_{SU} ns before LATCH goes low and held t_{HL} ns after LATCH goes high. While LATCH is low, the user should not change the data control inputs at B0, B1, and B2. The data control inputs at B0, B1, and B2, may only be changed when LATCH is high. NSTAT supervision output is not controlled by the LATCH control input.



12-3526(F)

Figure 3. Timing Requirements

Electrical Characteristics (continued)

Switch Characteristics

Table 11. Break Switches (SW1, 2)

Parameter	Min	Typ	Max	Unit
Off State:				
Maximum Differential Voltage	—	—	±320[1]	V
dc Leakage Current (Vsw = ±320 V)	—	—	±20	µA
On State (see On-State I-V Switch Characteristics section):				
Resistance	—	18	28	Ω
Maximum Differential Voltage (V_{MAX})[2]	—	—	320	V
Foldback Voltage Breakpoint 1 (V1)	72	—	—	V
Foldback Voltage Breakpoint 2 (V2)	V1 + 0.5	—	—	V
dc Current Limit 1 ($I_{LIMIT}1$)	105	250	450	mA
dc Current Limit 2 ($I_{LIMIT}2$)	2	—	—	mA
Dynamic Current Limit				
10 x 700 µs, 1000 V Applied Surge T < 0.5 µs	—	2.5	—	A
dV/dT Sensitivity[2, 3]	—	200	—	V/µs

1. At 25 °C, maximum voltage rating has a temperature coefficient of 0.167 V/°C.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dT sensitivity.

Table 12. Ring Return Switch (SW3)

Parameter	Min	Typ	Max	Unit
Off State:				
Maximum Differential Voltage	—	—	±320[1]	V
dc Leakage Current (Vsw = ±320 V)	—	—	±20	µA
On State (see On-State Switch I-V Characteristics section):				
Resistance	—	60	100	Ω
Maximum Differential Voltage (V_{MAX})[2]	—	—	130	V
dc Current Limit	—	200	—	mA
Dynamic Current Limit				
10 x 700 µs, 1000 V Applied Surge T = 0.5 µs	—	2.5	—	A
dV/dT Sensitivity[2, 3]	—	200	—	V/µs

1. At 25 °C, maximum voltage rating has a temperature coefficient of 0.167 V/°C.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dT sensitivity.

Electrical Characteristics (continued)

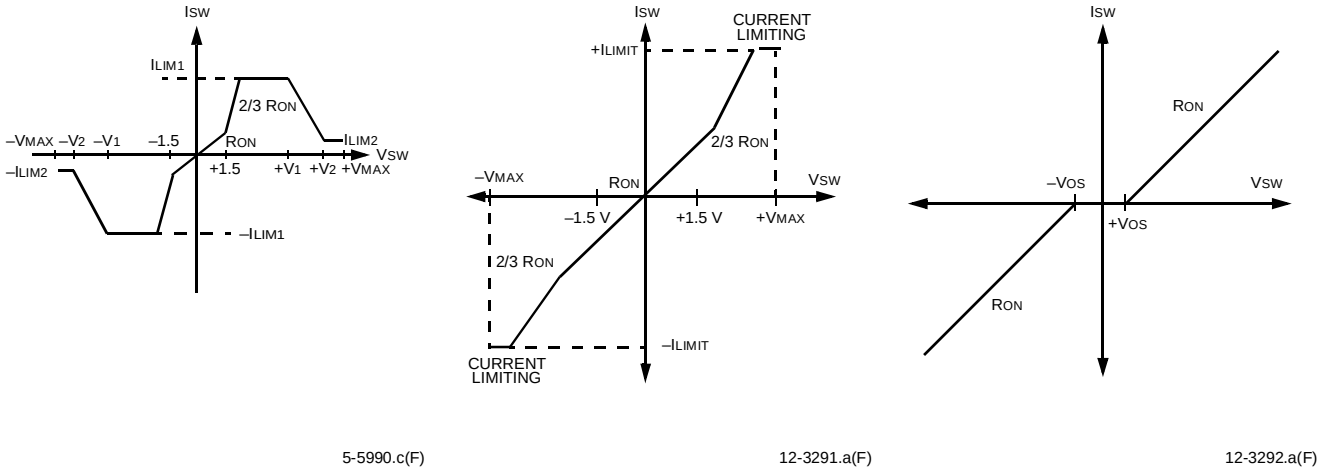
Switch Characteristics (continued)

Table 13. Ringing Access Switch (SW4)

Parameter	Min	Typ	Max	Unit
Off State:				
Maximum Differential Voltage	—	—	±475	V
dc Leakage Current (Vsw = ±475 V) (pole to pole)	—	—	±20	µA
Isolation	—	—	±320	V
On State (see On-State Switch I-V Characteristics section):				
Resistance	—	—	15	Ω
Voltage	—	—	3	V
Steady-state Current[1]	—	—	150	mA
Surge Current (10 x 700 µs pulse)[2]	—	—	2	A
Release Current	—	500	—	µA
dV/dT Sensitivity[2, 3]	—	200	—	V/µs

1. Choice of secondary protector and feed resistor should ensure these ratings are not exceeded. A minimum 400 Ω feed resistor is recommended.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dT sensitivity.

On-State Switch I-V Characteristics



A. Line Break Switch SW1, SW2 **B. Ring Return SW3** **C. Ring Access SW4**

Figure 4. On-State Switch I-V Characteristics

Test Configurations

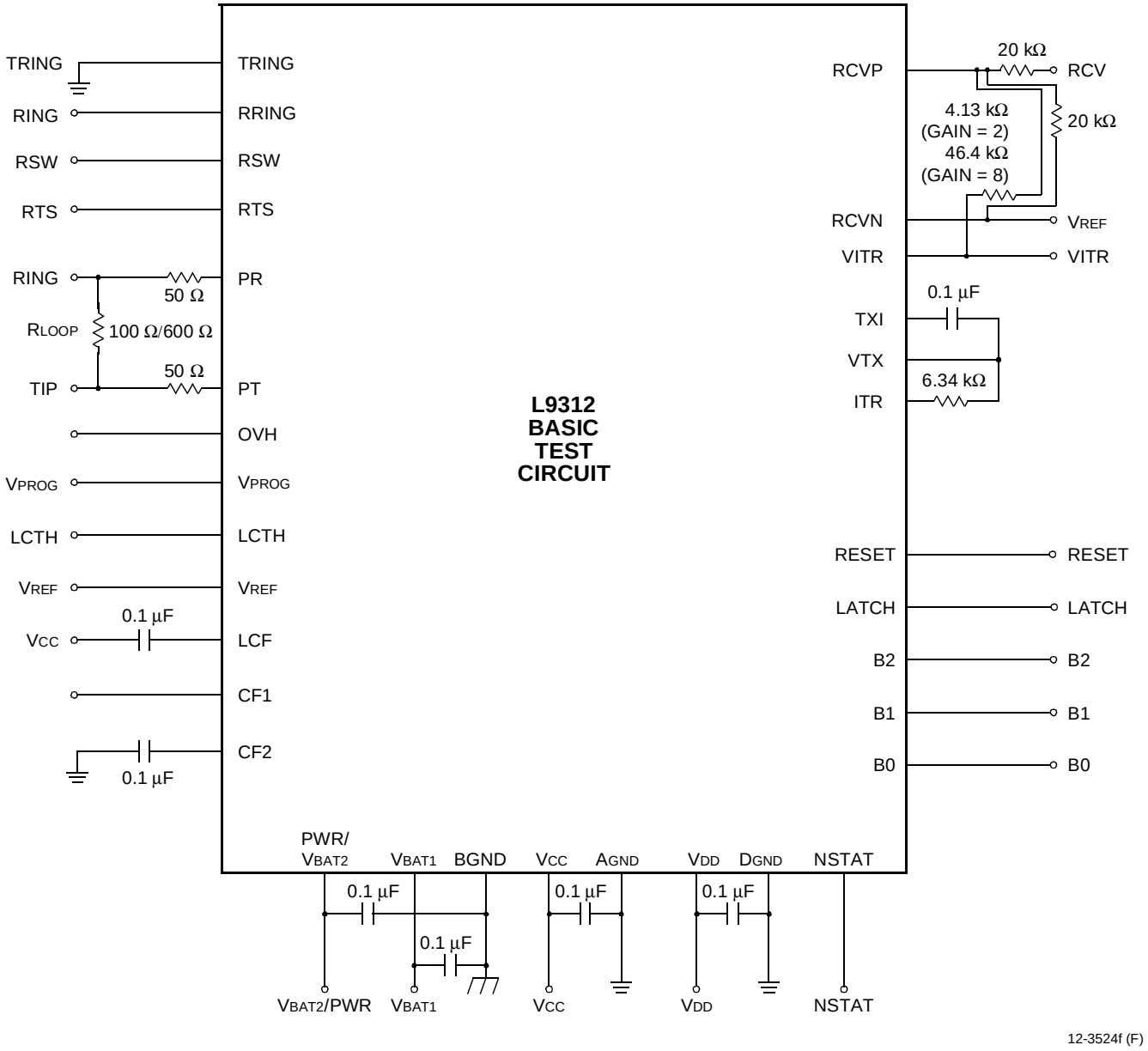
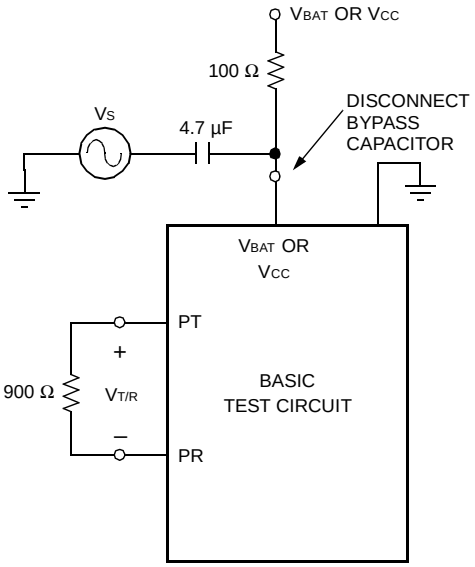


Figure 5. Basic Test Circuit

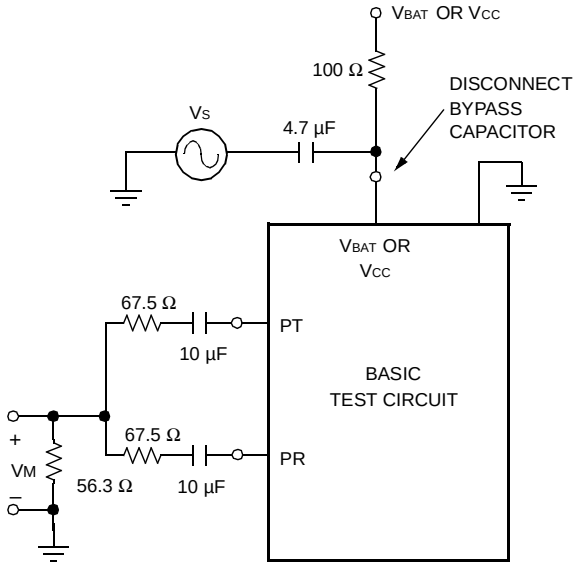
Test Configurations (continued)



$$PSRR = 20 \log \frac{V_S}{V_{T/R}}$$

12-2582 (F)

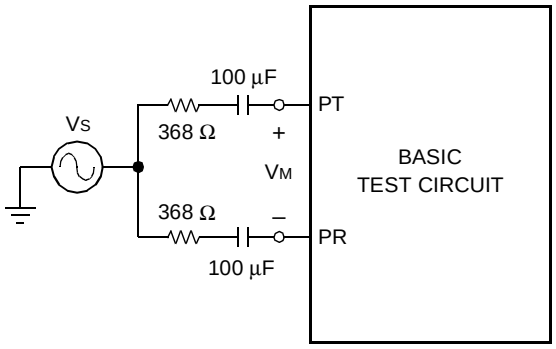
Figure 6. Metallic PSRR



$$PSRR = 20 \log \frac{V_S}{V_M}$$

12-2583 (F)

Figure 7. Longitudinal PSRR

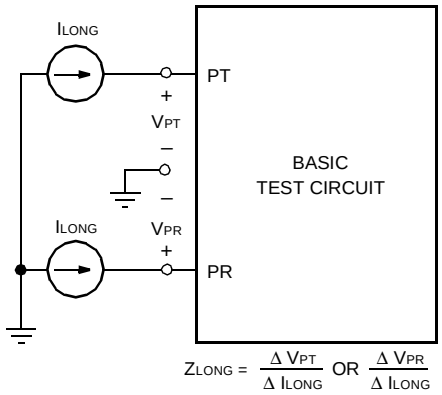


$$LONGITUDINAL\ BALANCE = 20 \log \frac{V_S}{V_M}$$

*ANSI**/*IEEE* STANDARD 455-1985

12-2584 (F)

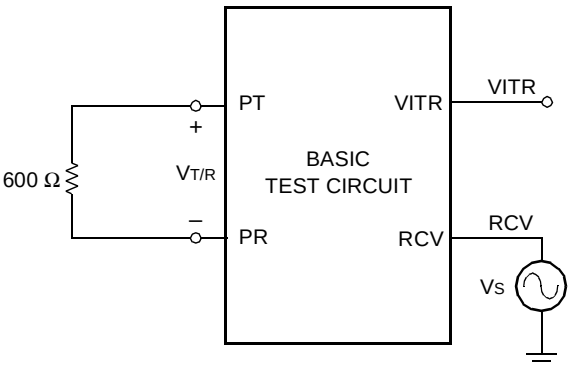
Figure 8. Longitudinal Balance



$$Z_{LONG} = \frac{\Delta V_{PT}}{\Delta I_{LONG}} \text{ OR } \frac{\Delta V_{PR}}{\Delta I_{LONG}}$$

12-2585 (F)

Figure 9. Longitudinal Impedance



$$G_{XMT} = \frac{VITR}{V_{T/R}}$$

$$G_{RCV} = \frac{V_{T/R}}{V_{RCV}}$$

12-2587.g (F)

Figure 10. ac Gains

* *ANSI* is a registered trademark of the American National Standards Institute, Inc.

Applications

dc Characteristics

Power Control

Under normal device operating conditions, thermal design must ensure that the device temperature does not rise above the thermal shutdown. Power dissipation is highest with higher battery voltages, with higher current limit, and under shorter dc loop conditions. Higher ambient temperature will reduce thermal margin. Power control may be done in several ways, by use of the integrated automatic battery switch and a lower-voltage auxiliary battery or by use of a power control resistor with single battery operation. The thermal capability of the 44-pin PLCC package is sufficient to allow for single battery operation without the power control resistor when the device is used under lower-power operating conditions.

Power Derating

Operating temperature range, maximum current limit, maximum battery voltage, minimum dc loop length, and protection resistors' values, number of PCB board layers, and airflow, will influence the overall thermal performance. The still-air thermal resistance of the 44-pin PLCC package is typically 38 °C/W for a two-layer board with 0 LFPM airflow.

The L9312 will enter thermal shutdown at a temperature of 150 °C. The thermal design should ensure that the SLIC does not reach this temperature under normal operating conditions.

For this example, assume a maximum ambient operating temperature of 85 °C, a maximum current limit of 30 mA, and a maximum battery of –56 V. Further assume a (worst-case) minimum dc loop of 20 Ω for wire resistance, 50 Ω protection resistors, and 200 Ω for the handset. Include the effects of parameter tolerance in these calculations.

$T_{TSD} – T_{AMBIENT(max)}$ = allowed thermal rise
150 °C – 85 °C = 65 °C

Allowed thermal rise =
package thermal impedance x SLIC power dissipation
65 °C = 38 °C/W x SLIC power dissipation

Allowed SLIC power dissipation (P_D) = 1.71 W

Thus, in this example, if the total power dissipated on the SLIC is less than 1.71 W, it will not enter thermal shutdown. Total SLIC power is calculated:

Total P_D = maximum battery x (maximum current limit) (current limit accuracy) + SLIC quiescent power.

For the L9312, the worst-case SLIC on-hook active quiescent power is 100 mW. Thus,

Total off-hook power = $(I_{LOOP})(1.05)$ x $(V_{BATAPPLIED})$ + SLIC quiescent power
Total off-hook power = (0.030 A)(1.05) x (52) + 100 mW
Total off-hook power = 1.864 W

The power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

SLIC P_D = total power – loop power

Loop off-hook power = $(I_{LOOP} \times 1.05)^2$ x $(R_{LOOPdcmin} + 2R_P + R_{HANDSET})$
Loop off-hook power = $\{(0.030\ A)(1.05)\}^2$ x
(20 Ω + 100 Ω + 200 Ω)
Loop off-hook power = 317.5 mW

SLIC off-hook power = total off-hook power – loop off-hook power
SLIC off-hook power = 1.864 W – 0.3175 W
SLIC off-hook power = 1.5465 W < 1.71 W

Thus, under the operating conditions of this example, the thermal capability of the 44-pin PLCC package is adequate to ensure that the L9312 will not be driven into thermal shutdown and no additional power control measures are needed. If, however, for a given set of operating conditions, the thermal capabilities of the package are not adequate to ensure the SLIC is driven into thermal shutdown, then one of the power control techniques described below should be used. Additionally, even if the thermal capability of the 44-pin PLCC package is adequate to ensure that the L9312 will not be driven into thermal shutdown, the battery switch technique described below can be used to reduce total short-loop power dissipation.

Automatic Battery Switch

Use of the automatic battery switch controls power dissipation by automatically switching to the lower-voltage auxiliary battery under short dc loop conditions, thus reducing the short-loop power that is generated. This has the advantage of not only controlling device temperature rise, but reducing overall power dissipation. The switch will automatically apply the appropriate battery to support the dc loop. No logic control is needed to control the switch. Switching is quiet, and the dc loop current will not be interrupted when switching between batteries. The lower-voltage auxiliary battery is connected to the V_{BAT2}/PRW package pin.

Applications (continued)

dc Characteristics (continued)

Automatic Battery Switch (continued)

The equation governing the switch point is as follows:

$$R_{LOOP} = \frac{|V_{BAT2}| - 3.0}{I_{LIM}} - 2R_P - R_{dc}$$

A graph showing loop and battery current versus loop resistance with use of the battery switch is shown in Figure 11.

The V_{BAT2} voltage must be chosen properly so that the power dissipation is minimized. When the voltage at pin PR equals V_{BAT2} + 1 V + (50 Ω x I_{LOOP}), at least 98% of the loop current minus 2.5 mA flows into V_{BAT2} and 2.5 mA + 2% of the loop current plus quiescent current flows into V_{BAT1}.

To choose V_{BAT2}, add:

1. Maximum tip overhead voltage (2 V for V_{OVH} = 0).
2. Maximum loop voltage (maximum loop resistance, protection resistance, and dc feed resistance [100 Ω] times the maximum loop current limit).
3. 1 V for the soft switch.

Thus, for a 40 mA current limit, 640 Ω loop, 30 Ω protection resistors, and 3.17 dBm signal (V_{OVH} = 0):

V_{BAT2} = –(2 + 0.042 x (100 + 60 + 640) + 1) = –36.6 V

Then, for any loop resistance from 0 Ω to 640 Ω, the worst-case V_{BAT1} and V_{BAT2} currents will be:

I_{BAT1} = 1.39 mA + 2.5 mA + 0.02 x (42 mA – 2.5 mA) = 4.68 mA

I_{BAT2} = (0.98) x 42 mA = 38.71 mA

Total max power = 1.641 W (V_{BAT} = –48 V)

Note that to minimize power statistically, this may not be the best choice for V_{BAT2}. Over a large number of lines, power is minimized according to the statistical distribution of loop resistance.

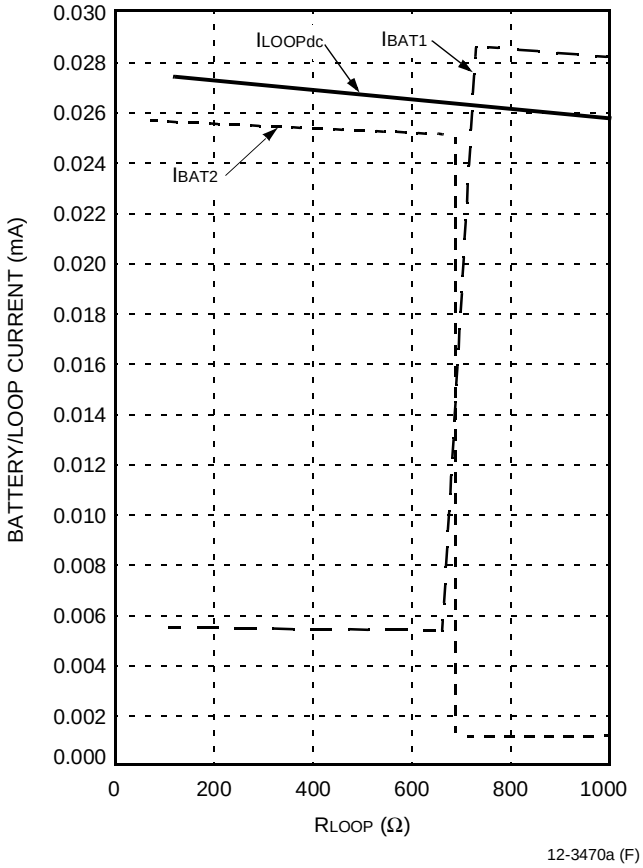


Figure 11. L9312 Loop/Battery Current (with Battery Switch) vs. Loop Resistance

Power Control Resistor

Device temperature rise may be controlled with use of a single battery voltage by use of a power control resistor. This technique will reduce power dissipation on the chip, by sharing the total power not dissipated in the loop between the L9312 and the power control resistor. It does not, however, reduce the total power consumed, as does use of the auxiliary battery. The power control resistor is connected from the primary battery to the V_{BAT2}/PWR node of the device.

The magnitude of the power control resistor must be low enough to ensure that sufficient power is dissipated on the resistor to ensure the L9312 does not exceed its thermal shutdown temperature. At the same time, the more power that is dissipated by the power control resistor, the higher the resistor's power rating must be, and thus, the more costly the resistor. The following equations are used to optimize the choice (magnitude and power rating) of the power control resistor.

Applications (continued)

dc Characteristics (continued)

Power Control Resistor (continued)

Again assume:

$T_{TSD} - T_{AMBIENT(max)}$ = allowed thermal rise
150 °C – 85 °C = 65 °C

Allowed thermal rise =
package thermal impedance x SLIC power dissipation
65 °C = 38 °C/W x SLIC power dissipation

Allowed SLIC power dissipation (P_D) = 1.71 W

This time, assume a maximum ambient operating temperature of 85 °C, a maximum current limit of 45 mA (including tolerance), and a maximum battery of –56 V.

Again, assume a (worst-case) minimum dc loop of 0 Ω and that 50 Ω protection resistors are used. Assume the handset is 200 Ω:

Total P_D = (56 V x 45 mA) + 0.100 W
Total P_D = 2.34 W + 0.100 W
Total P_D = 2.4375 W

Again, the power dissipated in the SLIC is the total power dissipation less the power that is dissipated in the loop.

SLIC P_D = total power – loop power

Loop power = $(I_{LIM})^2$ x ($R_{LOOPdcmin}$ + 2R_P + $R_{HANDSET}$)
Loop power = $(45\ mA)^2$ x (0 Ω + 100 Ω + 200 Ω)
Loop power = 0.6075 W

SLIC power = 2.4375 W – 0.6075 W
SLIC power = 1.83 W > 1.5 W

Under these extreme conditions, thermal margin is increased via an external power control resistor.

The power dissipated in the power control resistor is calculated by:

$$P_{PRW} = \frac{(|V_{BAT}| - V_{ROH} - V_{LOOP})^2}{R_{PWR}}$$

where in this example:

P_{PRW} is power in the resistor
V_{BAT} = –52 V
$V_{LOOP} = I_{LIM} * (R_{LOOP} + R_{PROT})$
V_{ROH} is the ring-side overhead voltage of the SLIC.

Since this device is dc unbalanced, the tip side overhead will remain typically at –2 V and the ring side overhead will vary with the voltage at V_{OH}. For the total tip/ring default overhead of 5.5 V, the ring overhead is typically 3.5 V.

Overhead Voltage

Overhead is programmable in the active mode via an applied voltage source at the device's OVH control input. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output or an external voltage source. A programmable external voltage source may be used to provide software control of the overhead voltage.

The overhead voltage (V_{OH}) is related to the OVH voltage by:

V_{OH} = 5.5 V + 5 x V_{OVH} (V)

Overall accuracy is determined by the accuracy of the voltage source and the accuracy of any external resistor divider network used and voltage offsets due to the specified input bias current. If a resistor divider from V_{REF} is used, lower magnitude resistor will give a more accurate result due to a lower offset associated with the input bias current; however, lower value resistors will also draw more power from V_{REF}. The sum of programming resistors should be between 75 kΩ and 200 kΩ.

Note that a default overhead voltage of 5.5 V is achieved by shorting input pin OVH to analog ground. Internally, the SLIC needs typically 2 V from each supply rail to bias the amplifier circuitry. This can be thought of as an internal saturation voltage.

The default overhead provides sufficient headroom for on-hook transmission of a 3.14 dBm signal into 900 Ω.

$$3.14 = 10 \log \frac{V^2}{0.9}$$

V = 1.36 V, which is required over and above the internal saturation voltage for signal swing.

1.36 V + 4 V = 5.36 V < 5.5 V default overhead; thus, a 3.14 dBm into 900 Ω signal is passed without clipping distortion.

The overhead voltage accuracy achieved will not only be affected by the accuracy of the internal SLIC circuitry, but also by the accuracy of the voltage source and the accuracy of any external resistor divider network used.

Applications (continued)

dc Characteristics (continued)

dc Loop Current Limit

In the active modes, dc current limit is programmable via an applied voltage source at the device's V_{PROG} control input. The voltage source may be an external voltage source or derived via a resistor divider network from the V_{REF} SLIC output or an external voltage source. A programmable external voltage source may be used to provide software control of the loop current limit. The loop current limit (I_{LIM}) is related to the V_{PROG} voltage by:

I_{LIM} (mA) = 50 x V_{PROG} (V)

Note that the overall current-limit accuracy achieved will not only be affected by the specified accuracy of the internal SLIC current-limit circuit (accuracy associated with the 50 term), but also by the accuracy of the voltage source and the accuracy of any external resistor divider network used and voltage offsets due to the specified input bias current. If a resistor divider from V_{REF} is used, a lower magnitude resistor will give a more accurate result due to a lower offset associated with the input bias current; however, lower value resistors will also draw more power from V_{REF}. The sum of the two resistors in the resistor divider should be between 75 kΩ and 200 kΩ. Offset at V_{PROG} and V_{REF} accuracies are specified in Table 6.

The above equation describes the active mode steady-state current-limit response. There will be a transient response of the current-limit circuit (with the device in the active mode) upon an on- to off-hook transition. Typical active mode transient current-limit response is given in Table 14.

Table 14. Typical Active Mode On- to Off-Hook Tip/Ring Current-Limit Transient Response

Parameter	Value	Unit
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 5 ms	I_{LIM} + 60	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 50 ms	I_{LIM} + 20	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 300 ms	I_{LIM}	mA

The current limit with the SLIC set in an active mode will be different from the current limit with the SLIC set in the scan mode. This is due to differences in the scan clamp circuit versus the active tip/ring drive amplifiers. The scan mode current limit is fixed and is a function of the internal design of the scan clamp circuit. The steady-state scan mode current limit will be a typical 40 mA to 50 mA and may, over temperature and process, vary typically from 30 mA to 110 mA. The scan clamp current limit will typically settle to its steady-state value within 300 ms.

Loop Range

The dc loop range is calculated using:

$$R_L = \frac{|V_{BAT}| - V_{OH}}{I_{LOOP}} - 2R_P - R_{dc}$$

V_{BAT1} is used because we are calculating the maximum loop range. The loop resistance value where the device automatically switches to V_{BAT2} is calculated in the Automatic Battery Switch section of this data sheet.

Battery Feed

The L9312 operates in a dc unbalanced mode. In the forward active state, under open circuit (on-hook) conditions, with the default overhead chosen, the tip to ring voltage will be a nominal 5.5 V less than the battery. This is the overhead voltage. The tip and ring overhead is achieved by biasing ring a nominal 3.5 V above battery and by biasing tip a nominal 2.0 V below ground.

During off-hook conditions, some dc resistance will be applied to the subscriber loop as a function of the physical loop length, protection, and telephone handset. As the dc resistance decreases from infinity (on-hook) to some finite value (off-hook), the tip to ring voltage will decrease as shown in Figure 12.

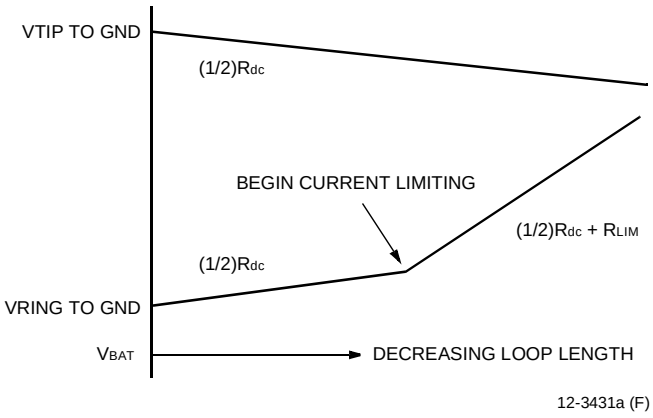


Figure 12. Tip/Ring Voltage

Applications (continued)

dc Characteristics (continued)

Battery Feed (continued)

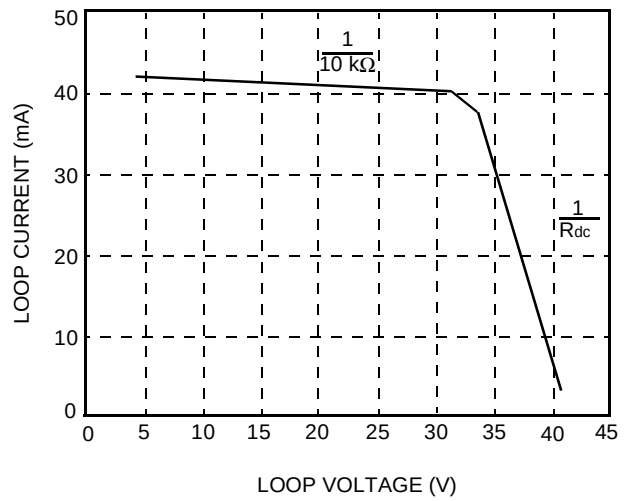
As illustrated in Figure 12, as loop length decreases, the tip to ground voltage will decrease with a slope corresponding to one-half the internal dc feed resistance of the SLIC (typical 75 Ω). The ring to ground voltage will also decrease with a slope corresponding to one-half the internal dc feed resistance of the SLIC, until the SLIC reaches the current-limit region of operation. At that point, the slope of the ring to ground voltage will increase to the sum of one half the internal dc feed resistance plus approximately 10 kΩ.

The dc feed characteristic can be described by:

$$I_{LOOP} = \frac{|V_{BAT}| - V_{OH}}{R_{LOOP} + 2R_P + R_{dc}}$$

$$V_{T/R} = \frac{(|V_{BAT}| - V_{OH}) \bullet R_{LOOP}}{R_{LOOP} + 2R_P + R_{dc}}$$

Where:
I_{LOOP} = dc loop current.
$V_{T/R}$ = dc loop voltage.
$|V_{BAT}|$ = battery voltage magnitude.
V_{OH} = overhead voltage.
R_{LOOP} = loop resistance, including wire and handset resistance.
R_P = protection resistance.
R_{dc} = SLIC internal dc feed resistance.



12-3050.g (F)

Notes:
V_{BAT1} = –48 V.

V_{BAT2} = –24 V.

I_{LIM} = 40 mA (R_{PROG} = 66.5 kΩ).

Figure 13. L9312 Loop Current vs. Loop Voltage

Refer to Figure 12 and Figure 13 in this section and to Figure 11 in the Automatic Battery Switch section.

Starting from the on-hook condition and going through to a short circuit, the curve passes through two regions:

Region 1: on-hook and low loop currents: the slope corresponds to the dc feed resistance of the SLIC (plus any series resistance). The open-circuit voltage is the battery voltage less the overhead voltage of the device.

Region 2: current limit: the dc current is limited to a value determined by V_{PROG}. This region of the dc template has a high resistance (10 kΩ).

Notice that the I-V curve is uninterrupted when the power is shifted from the high-voltage battery to the low-voltage battery (if auxiliary battery option is used).

This is shown in Figure 11 in the Automatic Battery Switch section.

Longitudinal to Metallic Balance

Longitudinal to metallic balance at PT/PR is specified in the Electrical Characteristics section of this data sheet.

Supervision

Loop Closure

Loop closure supervision threshold is programmed via an applied voltage source or ground, through a resistor at the LCTH input. Loop closure status is presented at the NSTAT output. NSTAT is an unlatched output that represents either the loop closure or ring trip status, depending on the device state. See Table 2 for more details. Loop closure threshold current (I_{LCTH}) is set by:

$$\frac{250(V_{REF} - V_{LCTH})}{R_{LCTH}\ (k\Omega)} = I_{LCTH}\ (mA)$$

where:
R_{LCTH} is a resistor from the LCTH node to ground or a voltage source.
V_{LCTH} is ground or an external voltage source.

There is a built-in hysteresis associated with the loop closure detector. The above equation describes the on-hook to off-hook threshold. To help prevent false glitches, the off-hook to on-hook threshold will be a typical 20% lower than the corresponding on-hook to off-hook threshold.

Supervision (continued)

Ring Trip

Ring trip is set by the value of RS1.

The ring trip threshold at the ring trip inputs is ±2.5 V minimum, ±3.5 V maximum.

A resistor value of 400 Ω, as shown in Figure 4, will set the ring trip current threshold to ±7.5 mA typical.

Ring trip is asserted upon entering the ringing mode until the second zero crossing of ringing. This is either a positive-going zero crossing (between –40 V and –30 V at –50 V V_{BAT}) or a negative-going zero crossing (between –10 V and –20 V at –50 V V_{BAT}). The different threshold for positive-going and negative-going zero crossings is the result of hysteresis of approximately 20 V. The act of turning on the switch may or may not produce a ringing zero crossing, therefore, there may be a delay of up to almost one cycle of ringing or 50 ms until NSTAT is high.

Ring trip will not be asserted unless the ring trip threshold is exceeded for two zero crossings. This is either a positive-going zero crossing (between –40 V and –30 V at –50 V V_{BAT}) or a negative-going zero crossing (between –10 V and –20 V at –50 V V_{BAT}). The different threshold for positive-going and negative-going zero crossings is the result of hysteresis of approximately 20 V.

Note that since the ringing voltage is monitored at RSW, one zero crossing can occur at switch turn-on depending on initial conditions.

Ring trip is asserted immediately if the ring trip input is 15 V ± 3 V.

Switching Behavior

The solid-state ring relay in the L9312 device is able to provide either make-before-break or break-before-make timing with respect to switching into and out of the ring mode. If switching is done directly into and out of the ring mode, the design of the L9312 will give make-before-break switching with respect to both the ring and tip side switches. To achieve break-before-make switching, the user should via software control enter an intermediate all-off mode when switching into and out of the ring mode. The all-off state should be held a minimum of 8 ms.

Make-Before-Break Operation

The break switches are constructed from DMOS transistors. The tip side ring return is also a DMOS transistor. Because the on resistance of the break switches is less than the tip side ring return switch, the break switches are physically bigger. This implies a larger gate to source capacitance, with inherently slower switching speeds since it will take longer to charge or discharge the gate to source capacitance of the break switches (to change the state of the switch). The ring access switch is a pnpn type device. The pnpn device has inherently faster switching speeds than any of the DMOS type switches.

Going from the active to ring mode, the smaller tip side ring return switch and the pnpn ring access switch will change states before the larger break switches. Thus, the ring contacts are made before the line break switches are broken: make-before-break operation.

Going from the ring mode to active or scan, the natural tendency is for the smaller tip side ring return DMOS to break or open, before the larger DMOS can turn on. This would not be make-before-break operation on the tip side. Thus, circuitry is added to speed up charging of the tip break switch, to speed up the turn on of that switch to give make-before-break operation on the tip side.

On the ring side, going from the ring mode to the active or scan mode, the pnpn will not turn off until the ring current drops below the hold current of the pnpn device (which is typically 500 μA); this is effectively zero current for zero current turn off. This can take up to one-half cycle of ringing to occur. With this inherent delay in switching by the pnpn ring access switch, the break switches will make contact before the ring access switch breaks contact; so again, make-before-break switching is achieved.

With the make-before-break switch, there will be a period of time (depending on ring signal frequency but measured in tens of microseconds) where all four switch contacts will be on. This means that the ring generator will be connected through the current-limited break switches to the input of the SLIC device. Current will be limited by the break switch current limit, and this will not damage the SLIC. This current may, however, cause a false glitch at the NSTAT supervision output that will need to be digitally filtered. The board designer should consider any ramifications of this state on the overall system or ring generator and battery design.

The major benefit of make-before-break switching is that it will minimize any impulse noise generated during ringing cadence. In many cases when operating the switch in the make-before-break mode, no special design to switch at zero current and voltage crossing is required. Impulse noise generation when using solid-state relays is documented in the *Impulse Noise and the L758X Series of Solid State Switches* Application Note.

Supervision (continued)

Break-Before-Make Operation

To achieve break-before-make, use the logic control sequence device switching as shown below.

Table 15. Break-Before-Make Logic Control Sequence Device Switching

State	Break Switches	Ring Switches	Comment
Active/Scan	closed	open	—
Disconnect (all-off)	open	open	hold >8 ms
Ring	open	closed	—
Disconnect (all-off)	open	open	hold >8 ms
Active/Scan	closed	open	—

The advantage of break-before-make operation is that it eliminates the current spike when the ring access relay changes state. The disadvantage is that it forces an all-off state. Under inductive ringing loads, due to Ldi/dt effects, it may cause a reduction in the impulse noise performance compared to make-before-break switching.

Protection

External Protection

An external overvoltage clamp is required to ensure that the off-state and on-state ratings of the solid-state break switch and solid-state ring access switch are not exceeded. The solid-state switches in the L9312 are constructed in a dielectrically isolated high-voltage technology. Because of the high device-to-device isolation that is inherent in the dielectric isolation, only a tip to ground and a ring to ground clamp is required. A tip to ring overvoltage clamp is not needed. A foldback or crowbar type device is recommended to minimize power across the solid-state switches under a fault condition.

The break switches and tip return switch are constructed from DMOS transistors. Because the on resistance of the break switches is less than the tip side ring return switch, the break switches are physically bigger and have a higher current handling capability. Additionally, the break switches have a foldback characteristic that enables them to survive a higher on-state voltage (320 V) than the tip ring return switch (130 V), which does not have the foldback characteristic. (See On-State Switch I-V Characteristics section.) The ring access switch is a pnpn type device. Additionally, the ring side will see the full power ring voltage, and the tip side switch will see the power ringing voltage that is attenuated by the ringing load, subscriber loop, feed resistor, and protection resistors. Because of these differences, the protection requirements on the tip side are different from the protection requirements on the ring side. Thus, it is recommended that an asymmetrical (with respect to tip and ring) overvoltage protection scheme be used.

Please contact your Agere Account Representative for a recommended protection device.

Additionally, a series protection resistor with a fusible characteristic or a PTC resistor is recommended to limit current during lightning and power cross faults. A minimum 50 Ω is recommended in tip and ring.

The overall device protection is achieved through a combination of the external overvoltage and overcurrent devices, along with the integrated thermal shutdown feature, the integrated window comparator, the break switch foldback characteristic, and the dc/dynamic current-limit response of the break and tip return switches.

Active Mode Response at PT/PR

The line break switches and tip return switch are current-limited switches. The current-limit mechanism limits current through the switch to the specified dc current limit under low frequency or dc faults (power cross and/or tip-ring to ground short) and limits the current to the specified dynamic current-limit response under transient faults, such as lightning.

During a lightning fault (typical 1000 V 10 x 700 µs applied surge), the current-limited line break switches will pass typically 2.5 A for 0.5 µs before forcing the break switches off. Once in the off state, the external protection device must ensure that the off-state voltage rating of 320 V is not exceeded. Note that the maximum differential voltage is the positive zener rating of the protection device less the battery voltage, which will appear on the line feed side of the switch.

Protection (continued)

Active Mode Response at PT/PR (continued)

For a lower-voltage power cross, whose maximum peak voltage is below the foldback voltage breakpoint 1 (V1), the current-limited break switch will pass the current equal to the dc current limit. The current limit has a negative temperate coefficient, so as the device continues to pass current, the current limit will reduce with increasing device temperature. Ultimately, the device will reach the thermal shutdown temperature and the thermal shutdown mechanism will force an all-off state, which will stop current flow and begin device cooling. In the all-off state, the external protection device ensures that the switch off-state voltage rating is not exceeded. Once the device cools significantly, the break switches will turn on, and current will begin to flow again, until temperature forces the all-off state. This will continue until the fault condition is gone.

Sneak-under surge is a voltage surge that is just below the clamping threshold of the secondary protection device. For this type of surge, when the surge voltage is below the foldback voltage breakpoint 1, operation is as described above. When the surge voltage rises above the foldback voltage breakpoint 1 (V1), but is still less than the secondary protector clamping voltage, the line break switch will crowbar into the high-impedance region of its I-V characteristic and reduce current to the specified $I_{LIMIT}2$ value.

For surges whose magnitude range above the trigger of the external secondary protector, the device will operate as described above for the portion of the surge below the secondary protector trigger voltage. When the voltage rises above the external secondary protector's trigger voltage, the secondary protector will crowbar on shunting fault current to ground and reducing the tip/ring voltage seen at the device.

In the active mode, the external secondary protector must ensure that the off-state voltage ratings of the ring access and ring return switch are not exceeded. Normally, the ring return switch is connected to ground on the TRING side and to the protector on the PT side; thus, the protector on the tip side in the active mode must clamp at less than 320 V. As will be seen in the Ring Mode Response at PT/PR section, during the power ringing mode, this clamp voltage on the tip side is significantly less than 320 V.

Normally, the ring access switch is connected to the ring generator on the RRING side and to the protector on the PR side; thus, on one side of the switch there is the battery voltage and the peak negative ring signal, and on the PR side, the maximum turn-on voltage of the secondary protector. The ring access switch is of pnpn construction. Thus, if the off-state voltage rating of the ring access switch is exceeded, the device will crowbar into a low-impedance state. This will cause a surge into the ring generator and can cause the on-state current rating of the switch to be exceeded.

The difference of the battery plus peak negative ring signal voltage less the maximum turn on of the secondary protector must not exceed the off-state voltage rating of the ring access switch. Additionally, as the secondary protector will see the power ring signal, the minimum turn-on rating of the secondary protector must be high enough to not clamp the ring signal and cause clipping distortion. The ring side will see the full-power ring voltage, and the tip side switch will see the power ringing voltage that is attenuated by the ringing load, subscriber loop, feed resistor, and protection resistors; thus, the ring side secondary protector requires a higher clamping voltage than the tip side.

Ring Mode Response at PT/PR

In this mode, the line break switches are off and the ring access and ring return switch is on. The secondary protectors must ensure that the minimum off-state voltage rating of the line break switches is not exceeded. Note that the maximum differential voltage is the positive zener rating of the protection device less the battery voltage which will appear on the line feed side of the switch.

The ring access switch is a pnpn type switch. This switch has no internal current limiting. Thus, through external current limit, the user must ensure that the surge ratings (both dynamic and dc for lightning and power cross faults) are not exceeded. A minimum 400 Ω ring feed resistor is recommended. This resistor also will set the ring trip threshold. See the Ring Trip section within the Supervision section of this data sheet.

During a lightning fault (typical 1000 V 10 x 700 µs applied surge), the current-limited tip return switch will pass, typically 2.5 A for 0.5 µs before forcing the switch off. Once in the off state, the external protection device must ensure that the off-state voltage rating of 320 V is not exceeded.

Protection (continued)

Ring Mode Response at PT/PR (continued)

For power cross for lower-voltage faults, the ring return switch will behave like the line break switches. However, tip return switch does not have the foldback clamping feature that is included in the line break switches; thus, in the on state, the voltage seen by the ring return switch before damage is less than the line break switches. The on-state voltage of the line break switches can go up to the off-state voltage rating. The ring return voltage should see less than 130 V in the on state. Thus, the secondary protector on the ring side should have a maximum crowbar voltage of 130 V. With typical protection device tolerance, this implies a minimum clamping voltage of 100 V. The users should ensure, based on minimum loop length, ringing load, and peak ring signal voltage, that the ring signal is not distorted by the (lower) voltage rating of the tip-side protector.

Internal Tertiary Protection

The external secondary protector and switch current limit protect the 320 V high-voltage switches from lightning and power cross conditions. Integrated into the LILAC IC is an internal tertiary protection scheme that is meant to protect the 90 V SLIC portion of the device from residue fault current and voltages that may be passed through the switches to the actual SLIC inputs. This scheme includes an internal diode bridge voltage clamp and a battery out of range detector that forces an all-off condition if the battery voltage falls high or low out of the specified operating range.

Diode Bridge

The internal inputs of the actual SLIC chip are clamped to ground and to V_{BAT1} by an integrated diode bridge. Residual positive fault currents are clamped to ground and residual negative fault currents are clamped to battery. This implies that the battery have some current sinking capability.

High common-mode currents, as may be seen under a fault condition, will be sensed and reduced to zero by the battery monitor circuit (see Battery Out of Range Detector: High [Magnitude] section). However, this detector will not prevent longitudinal current from flowing into battery. The battery supply must have the ability to sink longitudinal currents as specified in the longitudinal current capability requirement in Table 6.

Battery Out of Range Detector: High (Magnitude)

This feature is useful in remote power applications where a dc-dc converter with limited ability to sink current is used as the primary battery supply. Under a fault condition, the diode bridge will want to sink current into the battery. As a function of the dc-dc converter input capacitance and design, this current may cause the magnitude of supply voltage to rise and ultimately cause damage to the supply. To prevent damage to the supply, the LILAC device will monitor the battery supply voltage. If the magnitude of the battery rises above the maximum specified operating battery, the battery out of range detector will force the line break switches and ring access switches into an all-off state, and will also force the SLIC into the disconnect state. This will stop the current flow into the battery, preventing damage to the battery fault conditions. NSTAT is forced low during this mode of operation.

Battery Out of Range Detector: Low (Magnitude)

The LILAC device will monitor the battery supply voltage. If the magnitude of the battery drops below the minimum specified operating battery, the battery out of range detector will force the line break switches and ring access switches into an all-off state, and will also force the SLIC into the disconnect state. NSTAT is forced low during this mode of operation.

ac Applications

ac Parameters

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Transmit and receive gains may be specified in terms of an actual gain, or in terms of a transmission level point (TLP), that is, the actual ac transmission level in dBm. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

Codec Types

At this point in the design, the codec needs to be selected. The interface network between the SLIC and codec can then be designed. Below is a brief codec feature summary.

First-Generation Codecs. These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input stages, differential analog output stages, +5 V only or ±5 V operation, and μ-law/A-law selectability. These are available in single and quad designs. This type of codec requires continuous time analog filtering via external resistor/capacitor networks to set the ac design parameters. An example of this type of codec is the Agere T7504 quad 5 V only codec.

This type of codec tends to be the most economical in terms of piece part price, but tends to require more external components than a third-generation codec. Further ac parameters are fixed by the external R/C network so software control of ac parameters is difficult.

Third-Generation Codecs. This class of devices includes all ac parameters set digitally under microprocessor control. Depending on the device, it may or may not have data control latches. Additional functionality sometimes offered includes tone plant generation and reception, PPM generation, test algorithms, and echo cancellation. Again, this type of codec may be +5 V only or ±5 V operation, single quad or 16-channel, and μ-law/A-law or 16-bit linear coding selectable. Examples of this type of codec are the Agere T8536/7 (5 V only, quad, standard features), T8533/4 (5 V only, quad with echo cancellation), and the T8531/36 (5 V only, 16-channel with self-test).

ac Interface Network

The ac interface network between the L9312 and the codec will vary depending on the codec selected. With a first-generation codec, the interface between the L9312 and codec actually sets the ac parameters. With a third-generation codec, all ac parameters are set digitally, internal to the codec; thus, the interface between the L9312 and this type of codec is designed to avoid overload at the codec input in the transmit direction, and to optimize signal to noise ratio (S/N) in the receive direction.

Because the design requirements are very different with a first- or third-generation codec, the L9312 is offered with two different receive gains. Each receive gain was chosen to optimize, in terms of external components required, the ac interface between the L9312 and codec.

ac Applications (continued)

ac Interface Network (continued)

With a first-generation codec, the termination impedance is set by providing gain shaping through a feedback network from the SLIC VITR output to the SLIC RCVN/RCVP inputs. The L9312 provides a transconductance from T/R to VITR in the transmit direction and a single ended to differential gain in the receive direction, from either RCVN or RCVP to T/R. Assuming a short from VITR to RCVN or RCVP, the maximum impedance that is seen looking into the SLIC is the product of the SLIC transconductance times the SLIC receive gain, plus the protection resistors. The various specified termination impedance can range over the voiceband as low as 300 Ω up to over 1000 Ω. Thus, if the SLIC gains are too low, it will be impossible to synthesize the higher termination impedances. Further, the termination that is achieved will be far less than what is calculated by assuming a short for SLIC output to SLIC input. In the receive direction, in order to control echo, the gain is typically a loss, which requires a loss network at the SLIC RCVN/RCVP inputs, which will reduce the amount of gain that is available for termination impedance. For this reason, a high-gain SLIC is required with a first-generation codec.

With a third-generation codec, the line card designer has different concerns. To design the ac interface, the designer must first decide upon all termination impedance, hybrid balances, and TLP requirements that the line card must meet. In the transmit direction, the only concern is that the SLIC does not provide a signal that is too large and overloads the codec input. Thus, for the highest TLP that is being designed to, given the SLIC gain, the designer, as a function of voiceband frequency, must ensure the codec is not overloaded. With a given TLP and a given SLIC gain, if the signal will cause a codec overload, the designer must insert some sort of loss, typically a resistor divider, between the SLIC output and codec input.

In the receive direction, the issue is to optimize the S/N. Again, the designer must consider all the considered TLPs. The idea, for all desired TLPs, is to run the codec at or as close as possible to its maximum output signal, to optimize the S/N. Remember, noise floor is constant, so the larger the signal from the codec, the better the S/N. The problem is if the codec is feeding a high-gain SLIC, either an external resistor divider is needed to knock the gain down to meet the TLP requirements, or the codec is not operated near maximum signal levels, thus compromising the S/N.

Thus, it appears the solution is to have a SLIC with a low gain, especially in the receive direction. This will allow the codec to operate near its maximum output signal (to optimize S/N), without an external resistor divider (to minimize cost).

Note also that some third-generation codecs require the designer to provide an inherent resistive termination via external networks. The codec will then provide gain shaping, as a function of frequency, to meet the return loss requirements. Further stability issues may add external components or excessive ground plane requirements to the design.

To meet the unique requirements of both types of codecs, the L9312 offers two receive gain choices. These receive gains are mask programmable at the factory and are offered as two different code variations. For interface with a first-generation codec, the L9312 is offered with a receive gain of 8. For interface with a third-generation codec, the L9312 is offered with a receive gain of 2. In either case, the transconductance in the transmit direction, or the transmit gain, is 300 Ω.

This selection of receive gain gives the designer the flexibility to maximize performance and minimize external components, regardless of the type of codec chosen.

Design Tools

The following examples illustrate the design techniques/equations followed to design the ac interface with a first- or third-generation codec for both a resistive and complex design. To aid the line circuit design, Agere has available *Windows**-based spreadsheets to do the individual component calculations. Further, Agere has available *PSPICE*† models for circuit simulation and verification. Consult your Agere Account Representative to obtain these design tools.

First-Generation Codec ac Interface Network

Termination impedance may be specified as purely resistive or complex, that is, some combination of resistors and capacitors that causes the impedance to vary with frequency. The design for a pure resistive termination, such as 600 Ω, does not vary with frequency, so it is somewhat more straightforward than a complex termination design. For this reason, the case of a resistive design and complex design will be shown separately.

* *Windows* is a registered trademark of Microsoft Corporation.
† *PSPICE* is a registered trademark of MicroSim Corporation.

ac Applications (continued)

First-Generation Codec ac Interface Network: Resistive Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T7504 first-generation codec for a resistive termination impedance. For this example, the ac interface was designed for a 600 Ω resistive termination and hybrid balance with transmit gain and receive gain set to 0 dBm.

Also, this example illustrates the device with a single battery operation, fixed current limit, and fixed loop closure threshold. This is a lower feature application example.

Resistor R_{GN} is optional. It compensates for any mismatch of input bias voltage at the RCVN/RCVP inputs. If it is not used, there may be a slight offset at tip and ring due to mismatch of input bias voltage at the RCVN/RCVP inputs. It is very common to simply tie RCVN directly to ground in this particular mode of operation. If used, to calculate R_{GN}, the impedance from RCVN to ac ground should equal the impedance from RCVP to ac ground.

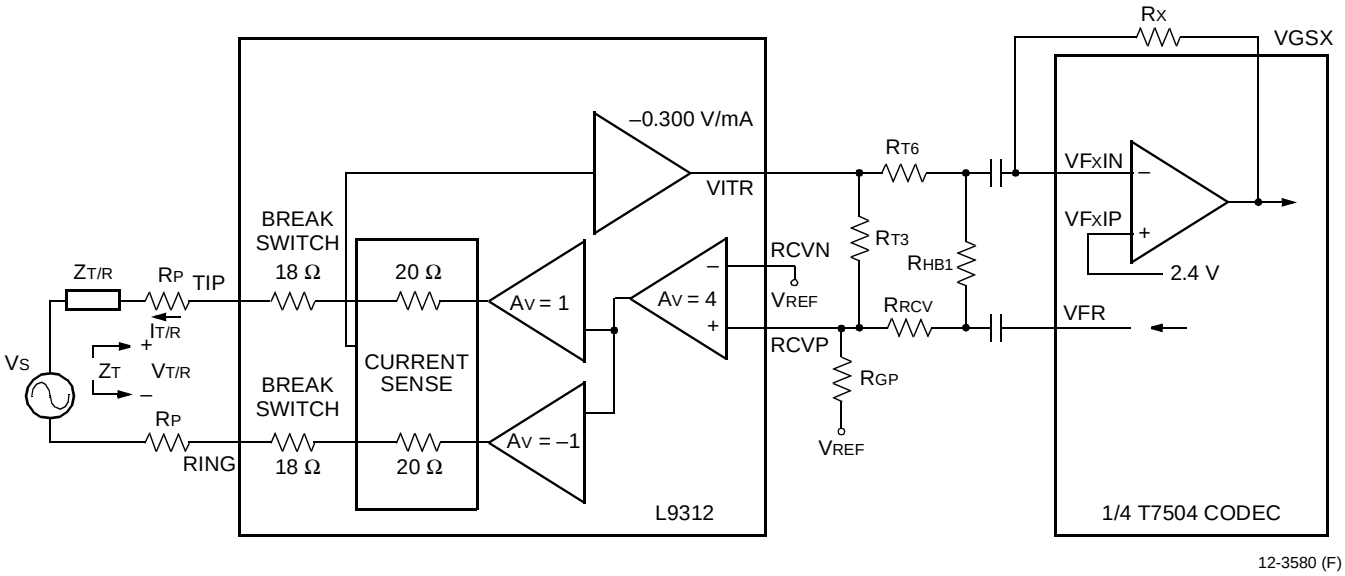


Figure 14. ac Equivalent Circuit

ac Applications (continued)

First-Generation Codec ac Interface Network: Resistive Termination (continued)

Example 1, Real Termination

The following design equations refer to the circuit in Figure 14. Use these to synthesize real termination impedance.

Termination Impedance:

$$Z_T = \frac{V_{T/R}}{-I_{T/R}}$$

$$Z_T = 76\ \Omega + 2R_P + \frac{2400}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}}$$

Receive Gain:

$$g_{rcv} = \frac{V_{T/R}}{V_{FR}}$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{Z_T}{Z_{T/R}}\right)}$$

Transmit Gain:

$$g_{tx} = \frac{V_{GSX}}{V_{T/R}}$$

$$g_{tx} = \frac{-R_X}{R_{T6}} \times \frac{300}{Z_{T/R}}$$

Hybrid Balance:

$$h_{bal} = 20 \log \left(\frac{R_X}{R_{HB1}} - g_{tx} \times g_{rcv}\right)$$

$$h_{bal} = 20 \log \left(\frac{V_{GSX}}{V_{FR}}\right)$$

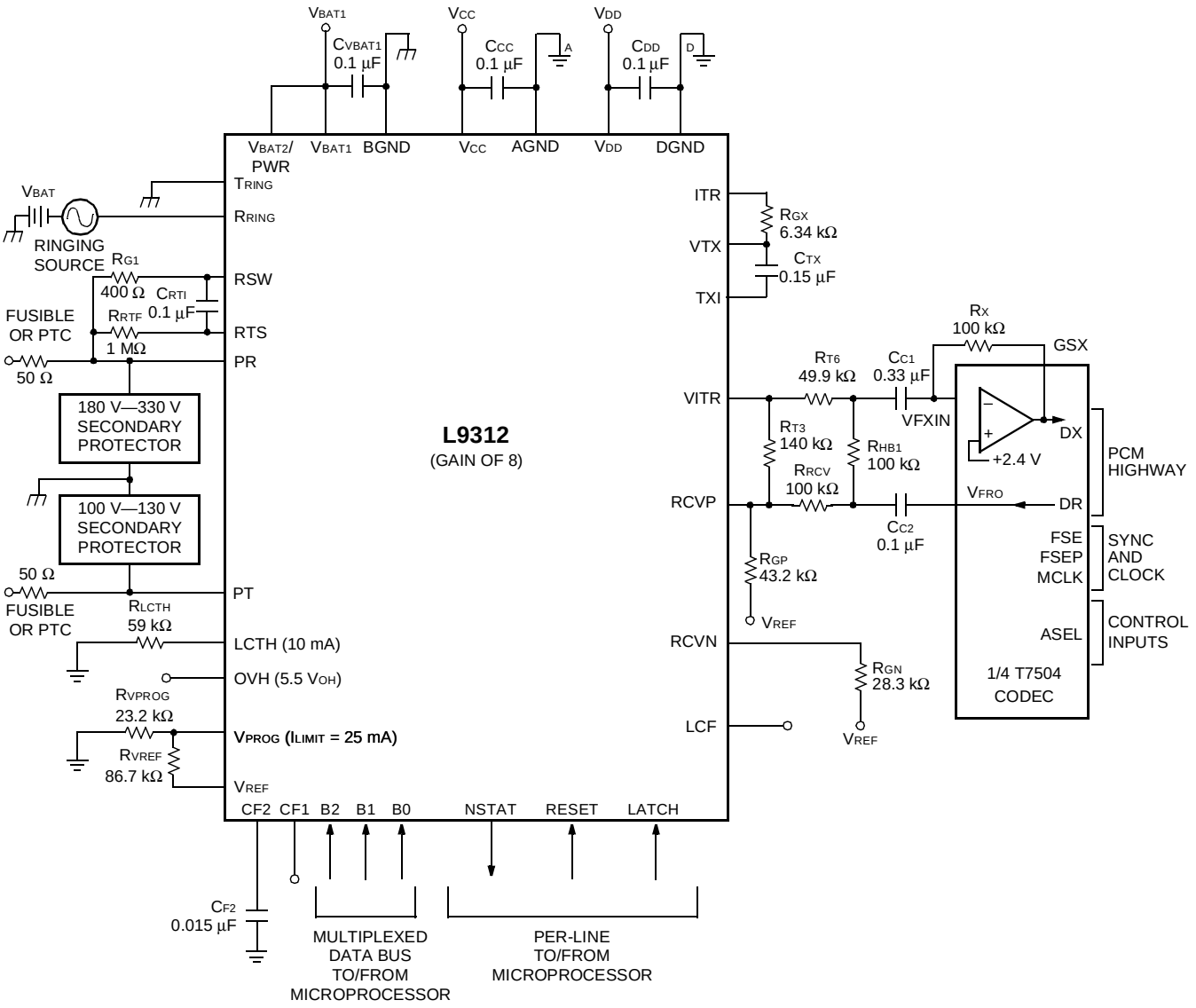
To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The expression for ZHB becomes:

$$R_{HB}(k\Omega) = \frac{R_X}{g_{tx} \times g_{rcv}}$$

ac Applications (continued)

First-Generation Codec ac Interface Network: Resistive Termination (continued)

Example 1, Real Termination (continued)



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Notes:
Termination impedance = 600 Ω.

Hybrid balance = 600 Ω.

Tx = 0 dBm.

Rx = 0 dBm.

Figure 15. Agere T7504 First-Generation Codec Resistive Termination, Single Battery Operation

ac Applications (continued)

First-Generation Codec ac Interface Network: Resistive Termination (continued)

Example 1, Real Termination (continued)

Table 16. L9312 Parts List for Agere T7504 First-Generation Codec Resistive Termination, Single Battery Operation

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PR}	50 Ω	1%	Fusible or PTC	Protection resistor.
R_{PT}	50 Ω	1%	Fusible or PTC	Protection resistor.
Protector*	180 V to 320 V	—	—	Ring-side secondary protector.
Protector*	100 V to 130 V	—	—	Tip-side secondary protector.
Power Supply				
C_{BAT1}	0.1 µF	20%	100 V	Filter capacitor.
C_{CC}	0.1 µF	20%	10 V	Filter capacitor.
C_{DD}	0.1 µF	20%	10 V	Filter capacitor.
C_{F2}	0.015 µF	20%	100 V	Filter capacitor.
dc Profile				
R_{VPROG}	23.2 kΩ	1%	1/16 W	With R_{VREF} fix dc current limit.
R_{VREF}	86.7 kΩ	1%	1/16 W	With R_{VPROG} fix dc current limit.
Supervision				
C_{RTF}	0.1 µF	20%	100 V	Ring trip filter capacitor.
R_{RTF}	1 MΩ	1%	1/16 W	Ring trip filter resistor.
R_{RS1}	400 Ω	5%	2 W	Sets ring trip threshold.
R_{LCTH}	59 kΩ	1%	1/16 W	With R_{VREF}, fix loop supervision threshold.
ac Interface				
R_{GX}	6.34 kΩ	1%	1/16 W	Sets T/R to VITR transconductance.
C_{TX}	0.15 µF	20%	10 V	ac/dc separation.
C_{C1}	0.33 µF	20%	10 V	dc blocking capacitor.
C_{C2}	0.1 µF	20%	10 V	dc blocking capacitor.
R_{T3}	140 kΩ	1%	1/16 W	With R_{GP} and R_{RCV}, sets termination impedance and receive gain.
R_{T6}	49.9 kΩ	1%	1/16 W	With R_X, sets transmit gain.
R_X	100 kΩ	1%	1/16 W	With R_{T6}, sets transmit gain.
R_{HB}	100 kΩ	1%	1/16 W	With R_X, sets hybrid balance.
R_{RCV}	100 kΩ	1%	1/16 W	With R_{GP} and R_{T3}, sets termination impedance and receive gain.
R_{GP}	43.2 kΩ	1%	1/16 W	With R_{RCV} and R_{T3}, sets termination impedance and receive gain.
R_{GN} Optional	28.3 kΩ	1%	1/16 W	Optional. Compensates for input offset at RCVN/RCVP.

* See your Agere Account Representative for a recommended secondary protection device.

ac Applications (continued)

Third-Generation Codec ac Interface Network: Complex Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T8536 third-generation. All ac parameters are programmed by the T8536. Note that this codec differentiates itself in that no external components are required in the ac interface to provide a dc termination impedance or for stability. Also, this example illustrates the device using the battery switch with multiple battery operation, programmable current limit, and programmable loop closure threshold. Please see the T8535/6 data sheet for information on coefficient programming.

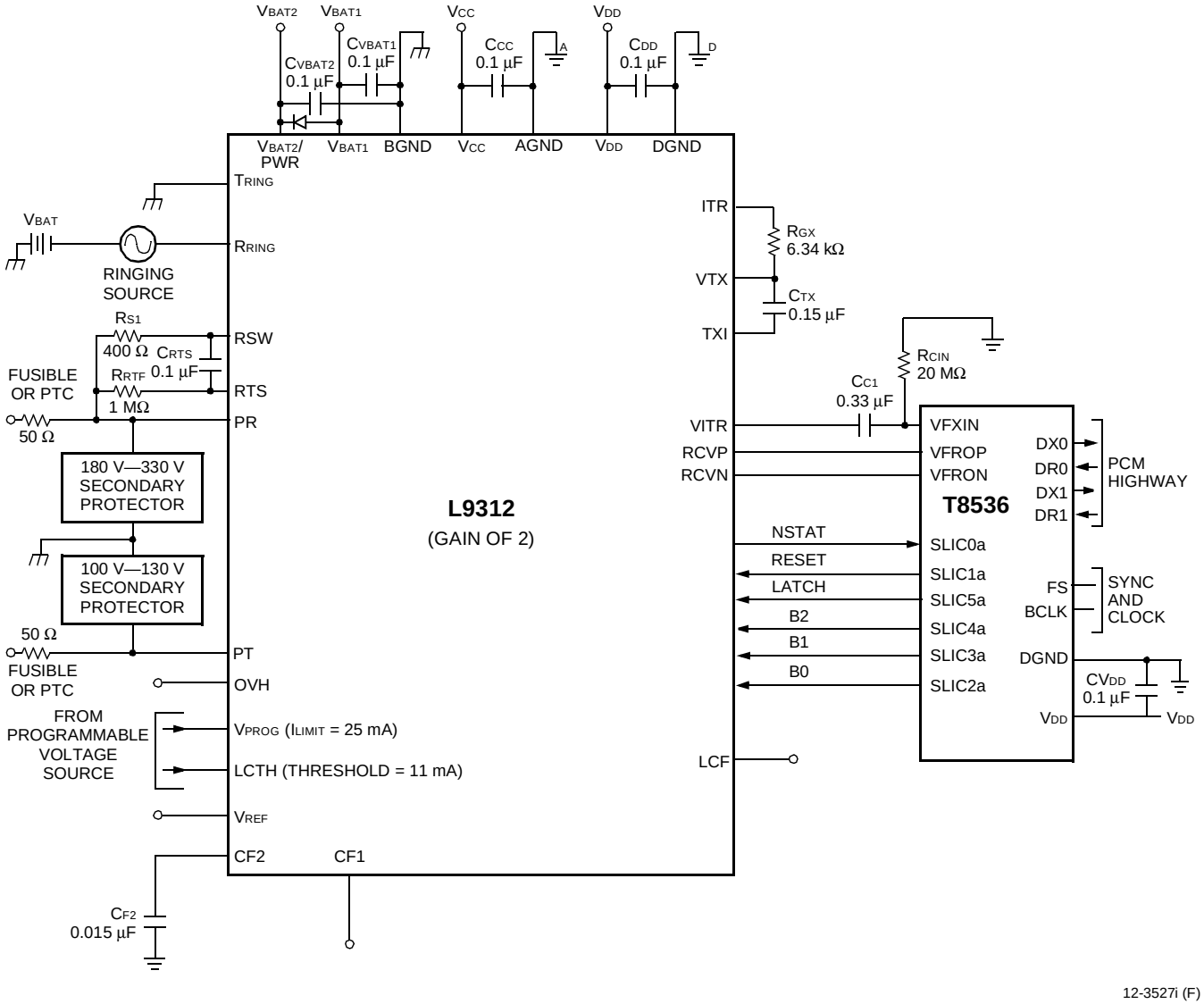


Figure 16. L9312 for Agere T8536 Third-Generation Codec, Dual Battery Operation, ac and dc Parameters, Fully Programmable

ac Applications (continued)

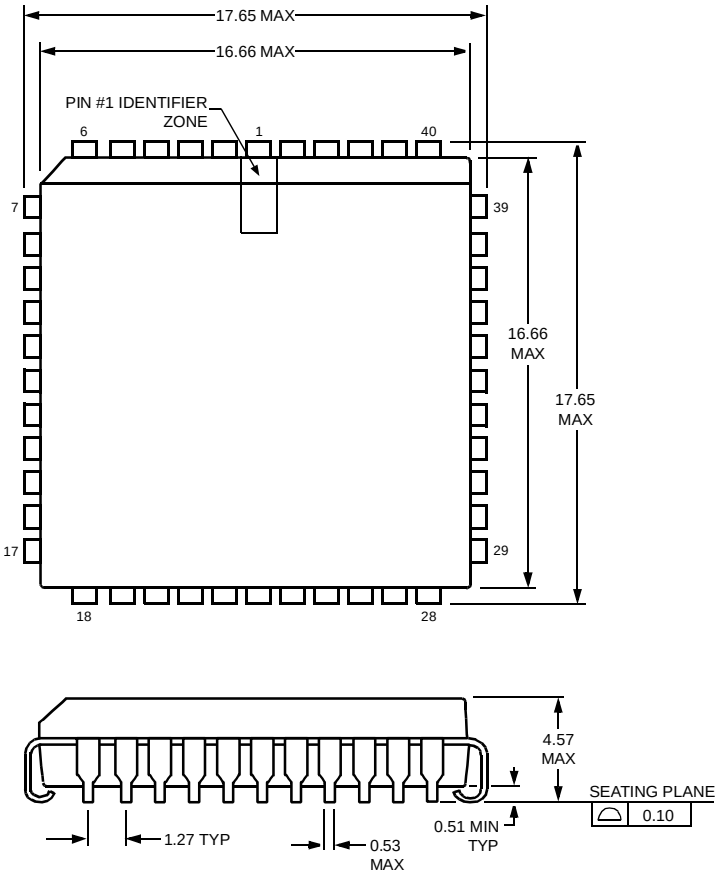
Third-Generation Codec ac Interface Network: Complex Termination (continued)

Table 17. L9312 Parts List for Agere T8536 Third-Generation Codec, Dual Battery Operation, ac and dc Parameters, Fully Programmable

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PR}	50 Ω	1%	Fusible or PTC	Protection resistor.
R_{PT}	50 Ω	1%	Fusible or PTC	Protection resistor.
Protector*	180 V to 320 V	—	—	Ring-side secondary protector.
Protector*	100 V to 130 V	—	—	Tip-side secondary protector.
Power Supply				
Diode	1N4004	—	—	Reverse battery current.
C_{BAT1}	0.1 µF	20%	100 V	Filter capacitor.
C_{BAT2}	0.1 µF	20%	50 V	Filter capacitor.
C_{CC}	0.1 µF	20%	10 V	Filter capacitor.
C_{DD}	0.1 µF	20%	10 V	Filter capacitor.
C_{F2}	0.015 µF	20%	100 V	Filter capacitor.
Supervision				
C_{RTF}	0.1 µF	20%	100 V	Ring trip filter capacitor.
R_{RTF}	1 MΩ	1%	1/16 W	Ring trip filter resistor.
R_{RS1}	400 Ω	5%	2 W	Sets ring trip threshold.
ac Interface				
R_{GX}	6.34 kΩ	1%	1/16 W	Sets T/R to VITR transconductance.
R_{CIN}	20 MΩ	5%	1/16 W	dc bias.
C_{TX}	0.15 µF	20%	10 V	ac/dc separation.
C_{C1}	0.33 µF	20%	10 V	dc blocking capacitor.

* See your Agere Account Representative for a recommended secondary protection device.

Outline Diagram



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Ordering Information

Device Part Number	Package	Comcode
LUCL9312AP-D	44-Pin PLCC, Dry-bagged	108698127
LUCL9312AP-DT	44-Pin PLCC, Dry-bagged, Tape and Reel	108698135
LUCL9312GP-D	44-Pin PLCC, Dry-bagged	108698200
LUCL9312GP-DT	44-Pin PLCC, Dry-bagged, Tape and Reel	108698218

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